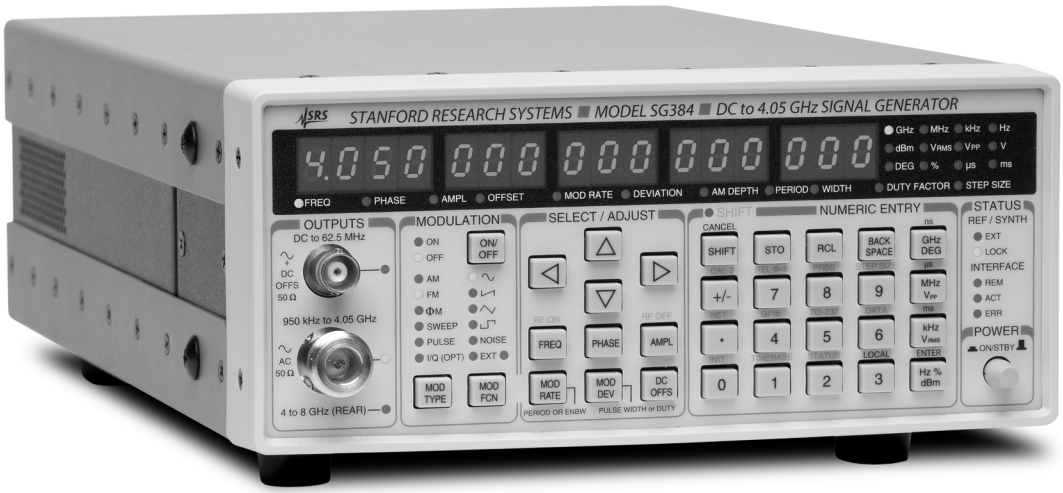
SG384

RF Signal Generator

User Manual



Stanford Research Systems

Revision 1.01

Certification

Stanford Research Systems certifies that this product met its published specifications at the time of shipment.

Warranty

This Stanford Research Systems product is warranted against defects in materials and workmanship for a period of one (1) year from the date of shipment.

Service

For warranty service or repair, this product must be returned to a Stanford Research Systems authorized service facility. Contact Stanford Research Systems or an authorized representative before returning this product for repair.

Stanford Research Systems, Inc.
1290-C Reamwood Avenue
Sunnyvale, California 94089
Phone: (408) 744-9040
Fax: (408) 744-9049
www.thinkSRS.com

Printed in the U.S

Contents

Contents i

Safety and Preparation for Use vii
Symbols You May Find on SRS Products viii
Specifications ix
Quick Start Instructions xvii

Introduction 1

Feature Overview 1
Waveform Overview 3
Spectral Overview 5
Front-Panel Overview 7
Parameter and Units Display 7
Main Output 8
Modulation Modes 9
Parameter Selection and Adjustment 10
Numeric Entry and Secondary Parameters 11
Power and Status 15
Rear-Panel Overview 16
AC Power 16
Timebase 16
Remote Interfaces 17
GPIB 17
RS-232 17
Ethernet 17
Modulation 17
Rear-Panel Optional Outputs 18
Option 1: Clock Outputs 18
Option 2: 8 GHz Frequency Doubler 18
Option 3: I/Q Modulator 18

Operation 19

Introduction 19
- Power-On 19
- Synthesizer and Outputs 20
- Setting Parameters 20
- Frequency 21
- Phase 21
- Amplitude and Power 22
- DC Offset 23
- RF ON/RF OFF 24

Sweeps and Modulation 25
- Introduction 25
- Modulation Rate 25
- Modulation Deviation 25
- Modulation Pane 26
  - Modulation On/Off 26
  - Modulation Type 26
  - Modulation Function 26
- Modulation Sources and Outputs 27
  - Linear Modulation 27
  - Pulse Modulation 27
  - Noise Modulation 28
  - Internal Modulation Source 28
- Amplitude Modulation 29
- Frequency Modulation 31
- Phase Modulation 35
- Pulse and Blank Modulation 37
- Phase Continuous Frequency Sweeps 39
- I/Q Modulation (Optional) 41

Secondary (Shift) Parameters 45
- REL Φ=0 45
- PRBS 45
- STEP SIZE 45
- Timebase 46
- NET 46
- GPIB 48
- RS-232 49
- DATA 49
- STATUS 50
- LOCAL 51
- INIT 51
- CAL 51

Factory Default Settings 52

Remote Programming 55

Introduction 55
Interface Configuration 55
GPIB 56
RS-232 56
LAN 57
Network Security 58
Front-Panel Indicators 58

Command Syntax 59
Parameter Conventions 60
Numeric Conventions 60

Abridged Index of Commands 61

Detailed Command List 63
Common IEEE-488.2 Commands 63
Status and Display Commands 66
Signal Synthesis Commands 69
Modulation Commands 72
List Commands 78
Interface Commands 79

Status Byte Definitions 81
Serial Poll Status Byte 81
Standard Event Status Register 82
Instrument Status Register 82

List Mode 83
List Instrument States 83
Enables/Disables 84
Modulation List States 85

Error Codes 87
Execution Errors 87
Query Errors 88
Device Dependent Errors 88
Parsing Errors 89
Communication Errors 90
Other Errors 90

Example Programming Code 91

Circuit Description 95

Overview 95
Block Diagram 95
Detailed Circuit Description 97
Front-Panel Display 98
Front-Panel Display Shield 98
Motherboard 99
Timebases 99
LF DDS and 19 MHz Reference 100
Microcontroller and Interface 101
Modulation Processor 102
Modulation ADC and DACs 103
RF DDS 104
RF Block and Rear-Panel Options Interface 105
Power Conditioning 106
Motherboard to RF Block Jumper 106
RF Output Block 106
RF Synthesizer 107
RF Dividers and Selectors 108
RF I/Q Modulator, Amplifiers and Attenuators 109
RF Output Attenuators 110
BNC Output 110
Power Supply 111
Rear-Panel Options 112
Clock Output (Options 1) 112
RF Doubler (Option 2) 113
I/Q Modulator (Option 3) 114
Timebase Options 114

Appendix A : Rational Approximation Synthesis 115

Phase Lock Loop Frequency Synthesizers 115
Phase Noise 116
Increasing Frequency Resolution 117
A Note on Fractional-N Synthesis 117
About YIG Oscillators 117
A New Approach 118
An Example 119
Elimination of Error 120
Conclusion 120

Appendix B : Parts List 121

Front-Panel Display (Assemblies 320) 123
Front-Panel EMI Filter (Assembly 324) 124
Motherboard (Assembly 322) 125
RF to Motherboard Jumper (Assembly 329) 132
RF Synthesizer (Assembly 327) 133
RF Output (Assembly 328) 136
Power Supply (Assembly 337) 138
Clock and 4 to 8 GHz Doubler (Option 1 & 2) (Assembly 332) 139
IQ Modulator (Option 3) (Assembly 335) 141
OCXO Timebase (Assembly 605) 142
Rubidium Timebase (Option 4) (Assembly 607) 142
Chassis (Assembly 336) 142

Appendix C : SG384 Schematic List 143

Schematic 1: Block Diagram 145
Schematic 2: Front Panel Display 146
Schematic 3: Display EMI Filter 147
Schematic 4: Mother Board 1, Frequency Refs 148
Schematic 5: Mother Board 2, 19 MHz Ref 149
Schematic 6: Mother Board 3, CPU 150
Schematic 7: Mother Board 4, Modulation Processor 151
Schematic 8: Mother Board 5, Modulation ADC / DACs 152
Schematic 9: Mother Board 6, RF Reference 153
Schematic 10: Mother Board 7, Interface 154
Schematic 11: Mother Board 8, Power Supplies 155
Schematic 12: Mother Board to RF Jumper 156
Schematic 13: Synthesizer 1, 2-4 GHz and Control 157
Schematic 14: Synthesizer 2, Dividers and LPF 158
Schematic 15: Output 1, Attenuation & Controls 159
Schematic 16: Output 2, RF Stage 160
Schematic 17: Output 3, BNC 161
Schematic 18: Power Supply 162
Schematic 19: Rear Panel Option Jumper 163
Schematic 20: Option #1 Clock Outputs 164
Schematic 21: Option #2 4-8 GHz Doubler 165
Schematic 22: Option #3 I/Q Modulator 166
Schematic 23: Timebase Adaptor Interface 167

Revisions 169

Safety and Preparation for Use

Line Voltage

The SG384 operates from a 90 to 132 V_{AC} or 175 to 264 V_{AC} power source having a line frequency between 47 and 63 Hz. Power consumption is less than 90 VA total. In standby mode, power is turned off to the main board. However, power is maintained at all times to the installed timebase. Units with standard ovenized quartz oscillator or optional rubidium timebase will consume less than 15 VA and 25 VA, respectively, in standby mode.

Power Entry Module

A power entry module, labeled AC POWER on the back panel of the SG384, provides connection to the power source and to a protective ground.

Power Cord

The SG384 package includes a detachable, three-wire power cord for connection to the power source and protective ground.

The exposed metal parts of the box are connected to the power ground to protect against electrical shock. Always use an outlet which has a properly connected protective ground. Consult with an electrician if necessary.

Grounding

BNC shields are connected to the chassis ground and the AC power source ground via the power cord. Do not apply any voltage to the shield.

Line Fuse

The line fuse is internal to the instrument and may not be serviced by the user.

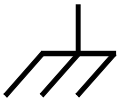
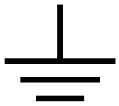
Operate Only with Covers in Place

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without all covers and panels in place.

Serviceable Parts

The SG384 does not include any user serviceable parts. Refer service to a qualified technician.

Symbols You May Find on SRS Products

Symbol	Description
	Alternating Current
	Caution – risk of electrical shock
	Frame or Chassis terminal
	Caution – refer to accompanying document
	Earth (ground) terminal
	Battery
	Fuse
	Power On
	Power Off
	Power Standby

Specifications

Frequency Setting (f_C)

Frequency ranges	
BNC output	DC to 62.5 MHz
N-type output	950 kHz to 4.05 GHz
SMA rear-panel (Option 2)	4.05 GHz to 8.1 GHz
Frequency resolution	1 µHz at any frequency
Switching speed	<8 ms (to within 1 ppm)
Frequency error	$<(10^{-18}$ + timebase error) × f_C
Frequency stability	$<1{:}10^{-11}$ (1 second Allan variance)

Spectral Purity of the RF Output Referenced to 1GHz (1)

Sub harmonics	None (No doublers are used below 4 GHz.)
Harmonics	<–25 dBc with <+7 dBm on N-Type output
Spurious	
offsets from carrier	
<10 kHz	<–65 dBc
≥10 kHz	<–75 dBc
Phase noise	
Offset from carrier	Phase Noise (typical)
10 Hz	–80 dBc/Hz
1 kHz	–102 dBc/Hz
20 kHz	–116 dBc/Hz
1 MHz	–130 dBc/Hz
Residual FM	1 Hz rms, typical, over 300 Hz to 3 kHz bandwidth
Residual AM	0.006 % rms, typical, over 300 Hz to 3 kHz bandwidth

(1) Spurs, phase noise and residual FM scale by 6 dB/octave to other carrier frequencies

Phase Setting of Front-Panel Outputs

Phase range	±360 °
Phase resolution	
DC to 100 MHz	0.01°
100 MHz to 1 GHz	0.1°
1 GHz to 8.1 GHz	1.0°

Timebase Input

Frequency	10 MHz, ±2 ppm
Amplitude	0.5 to 4 V_{PP} (–2 dBm to +16 dBm)
Input impedance	50 Ω, AC coupled

Timebase Output

Frequency	10 MHz, sine
Source	50 Ω, DC transformer coupled
Amplitude	1.75 V_{PP} ±10 % (8.8 ± 1 dBm)

Standard OCXO Timebase

Oscillator type	Oven controlled, 3rd OT, SC-cut crystal
Stability	<0.002 ppm (0 to 45°C)
Aging	<0.05 ppm/year

Rubidium Timebase (Option 4)

Oscillator type	Oven controlled, 3rd OT, SC-cut crystal
Physics package	Rubidium vapor frequency discriminator
Stability	<0.0001 ppm (0 to 45°C)
Aging	<0.001 ppm/year

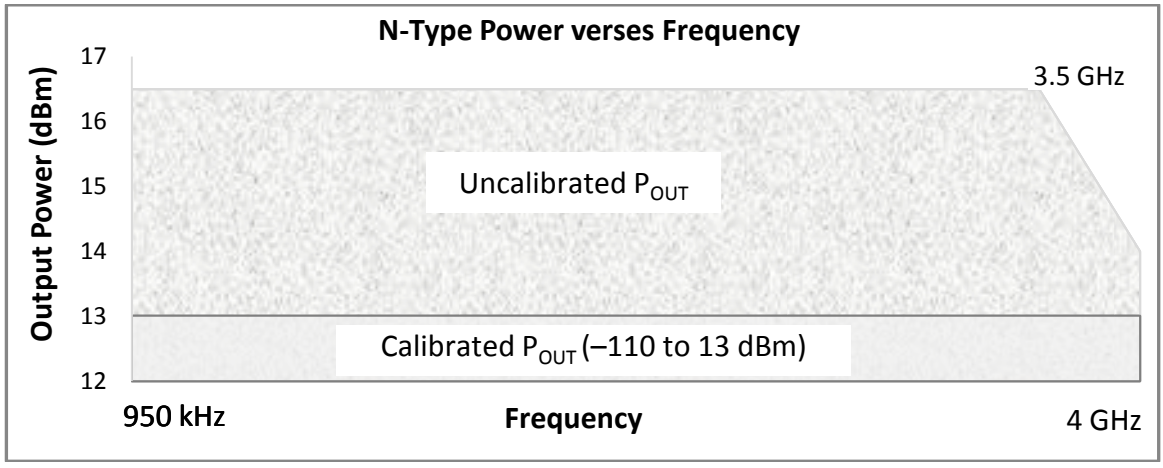
Front-Panel BNC Output (50 Ω load)

Frequency range	DC to 62.5 MHz
Amplitude	
Specified	1.00 to 0.001 V_{RMS} (+13 dBm to –47 dBm)
Allowed[1]	to 1.25 V_{RMS} (+14.96 dBm)
Offset	±1.5 V_{DC}
Maximum excursion	±1.42 V (amplitude + offset)
Amplitude resolution	<1 %
Amplitude accuracy	±5 %
Offset resolution	5 mV
Harmonics	<–40 dBc
Spurious	<–75 dBc
Output coupling	DC, 50 Ω ±2 %
User load	50 Ω
Reverse protection	±5 V_{DC}

Front-Panel N-type Output (50 Ω load)

Frequency range	950 kHz to 4.05 GHz
Power output	
Specified	+13 dBm to –110 dBm
Allowed [1]	16.5 dBm
Voltage output	
Specified	1 V_{RMS} to 0.7 μV_{RMS}
Allowed [1]	1.5 V_{RMS}
Power resolution	0.01 dBm
Power accuracy	±1 dB
Output coupling	50 Ω, AC
User load	50 Ω
VSWR	<1.6
Reverse protection	30 V_{DC}, +25 dBm RF

[1] Allowed power setting for which specifications are not guaranteed



Graph 1: N-Type Uncal'ed Power verses Frequency

Internal Modulation Source

Waveforms	Sine, ramp, saw, square, pulse, noise
Sine THD	–80 dBc (typical at 20 kHz)
Ramp linearity	<0.05 % (1 kHz)
Rate	
$f_C \leq$ 62.5 MHz	1 µHz to 500 kHz
$f_C >$ 62.5 MHz	1 µHz to 50 kHz
Rate resolution	1 µHz
Rate error	$<1:2^{31}$ + timebase error
Noise function	White Gaussian noise, RMS = DEV / 5
Noise bandwidth	1 µHz < ENBW < 50 kHz
Pulse generator period	1 µs to 10 s
Pulse generator width	100 ns to 9999.9999 ms
Pulse timing resolution	5 ns
Pulse noise function	PRBS length 2^5 to 2^{19}. Bit period (100 + n·5) ns 100 ns to 10 s in 5 ns steps

Modulation Waveform Output

Output impedance	50 Ω (for reverse termination)
User load	Unterminated 50 Ω coax
AM, FM, ΦM	±1 V for ± full deviation
Pulse/Blank	"Low" = 0 V, "High" = 3.3 V_{DC}
Connector	Rear-panel BNC

External Modulation Input

Modes	AM, FM, ΦM, Pulse and Blank
Unmodulated level	0 V input for unmodulated carrier
AM, FM, ΦM	±1 V input for ± full deviation
Modulation bandwidth	>100 kHz
Modulation distortion	<–50 dB
Input impedance	100 kΩ
Input Coupling	AC (4 Hz) or DC
Input offset	<500 µV
Pulse/Blank threshold	+1 V_{DC}
Connector	Rear-panel BNC

Frequency Modulation

Frequency deviation	
Minimum	0.1 Hz
Maximum	
$f_C \leq 126.5625$ MHz	1 MHz
$f_C \leq 253.1250$ MHz	2 MHz
$f_C \leq 506.25$ MHz	4 MHz
$f_C \leq 1.0125$ GHz	6 MHz
$f_C \leq 2.025$ GHz	16 MHz
$f_C \leq 4.050$ GHz	32 MHz
$f_C \leq 8.100$ GHz	64 MHz
Deviation resolution	0.1 Hz
Deviation accuracy	
$f_C \leq 62.5$ MHz	<0.1 %
$f_C > 62.5$ MHz	<3 %
Modulation source	Internal or external
Modulation distortion	<–70 dB (f_C = 1 GHz, f_M = 20 kHz, f_D = 20 kHz)
Ext FM carrier offset	<1:1000 of deviation
Modulation bandwidth	
$f_C \leq 62.5$ MHz	500 kHz
$f_C > 62.5$ MHZ	100 kHz

Phase Continuous Frequency Sweeps

Frequency span	0.1 Hz to entire sweep range
Sweep ranges	DC to 62.5 MHz
	59.375 to 128.125 MHz
	118.75 to 256.25 MHz
	237.5 to 512.5 MHz
	475 to 1025 MHz
	950 to 2050 MHz
	1900 to 4100 MHz
	3800 to 8200 MHz (Opt. 2 only)
Deviation resolution	0.1 Hz
Sweep source	Internal or external
Sweep distortion	<0.1 Hz + (deviation / 1000)
Sweep offset	<1:1000 of deviation
Sweep function	Triangle, ramps, or sine up to 120 Hz

Phase Modulation

Deviation	0 to 360°
Deviation resolution	
DC < f_C < 100 MHz	0.01°
100 MHz < f_C < 1 GHz	0.1°
$f_C > 1$ GHz	1.0°
Deviation accuracy	
$f_C \leq 62.5$ MHz	<0.1 %
$f_C > 62.5$ MHZ	<3 %
Modulation source	Internal or external
Modulation distortion	<–70 dB (f_C = 1 GHz, f_M = 20 kHz, Φ_D = 90°)
Modulation bandwidth	
$f_C \leq 62.5$ MHz	500 kHz
$f_C > 62.5$ MHZ	100 kHz

External I/Q Modulation (Option 3)

Carrier Frequency Range	Operates on 400 MHz ≤ f_C ≤ 4.05 GHz
Modulated output	Front-panel N-type only (+10 dBm max)
I/Q inputs	50 Ω, ±0.5 V, (rear BNCs)
I or Q input offset	<500 µV
I/Q full scale	$(I^2 + Q^2)^{1/2}$ = 0.5 V
Carrier suppression	>40 dBc
Modulation bandwidth	100 MHz

Amplitude Modulation

Range	0 to 100 % (Decreases above +7 dBm output)
Resolution	0.1 %
Modulation source	Internal or external
Modulation distortion (f_M = 1 kHz, Depth = 50%)	
f_C ≤ 62.5 MHz, BNC output	<1 %
f_C > 62.5 MHz, N-type output	<3 % typical
Modulation bandwidth	>100 kHz

Pulse/Blank Modulation

Pulse mode	Logic “high” turns BNC and RF on
Blank mode	Logic “high” turns BNC and RF off
On/Off ratio	
N-Type	
1 to 4 GHz	40 dB
Less than 1 GHz	60 dB
BNC	70 dB
Pulse feed-through	10 % of carrier for 20 ns at turn-on (typical)
Turn on/off delay	60 ns
RF rise/fall time	20 ns
Modulation source	Internal or external pulse

Square Wave Clock Outputs (Option 1)

Differential clocks	Rear-panel SMAs drive 50 Ω loads
Frequency range	DC to 4.05 GHz
Transition time	<35 ps (20 % to 80 %)
Jitter	
F_C> 62.5 MHz	<300 fs rms (1 kHz to 5 MHz BW)
F_C≤ 62.5 MHz	$<10^{-4}$ U.I. rms
Amplitude	0.4 to 1.0 V_{PP}
Offset	±2 V_{DC}
Amplitude & Offset resolution	5 mV
Amplitude & Offset accuracy	±5 %
Output coupling	DC, 50 Ω ± 2 %
Compliance	ECL, PECL, RSECL, CML & LVDS

RF Doubler Output (Option 2)

Output	Rear-panel SMA
Frequency range	4.05 to 8.10 GHz
RF amplitude	
4.05 to 7 GHz	–10 dBm to +13 dBm
7 to 8.10 GHz	–10 dBm to +7 dBm
Allowed [2]	+16.5 dBm
Sub harmonic (f_C / 2)	
$f_C < 6.5$ GHz	<–25 dBc typical
$f_C = 8.1$ GHz	<–12 dBc typical
Mixing products ($2f_C$ and $3f_C$ / 2)	<–20 dBc
Harmonics ($n \times f_C$)	<–25 dBc
Spurious (8 GHz)	<–55 dBc (> 10 kHz offset)
Phase noise (8 GHz)	–98 dBc/Hz at 20 kHz offset, typical
Amplitude resolution	0.01 dBm
Amplitude accuracy	
4.05 to 6.5 GHz	±1 dB
6.5 to 8.10 GHz	±2 dB
Modulation modes	FM, ΦM, and Sweeps
Output coupling	AC, 50 Ω
Reverse protection	30 V_{DC}, +25 dBm RF

[2] Allowed power setting for which specifications are not guaranteed

DC Bias Source (comes with Option 2)

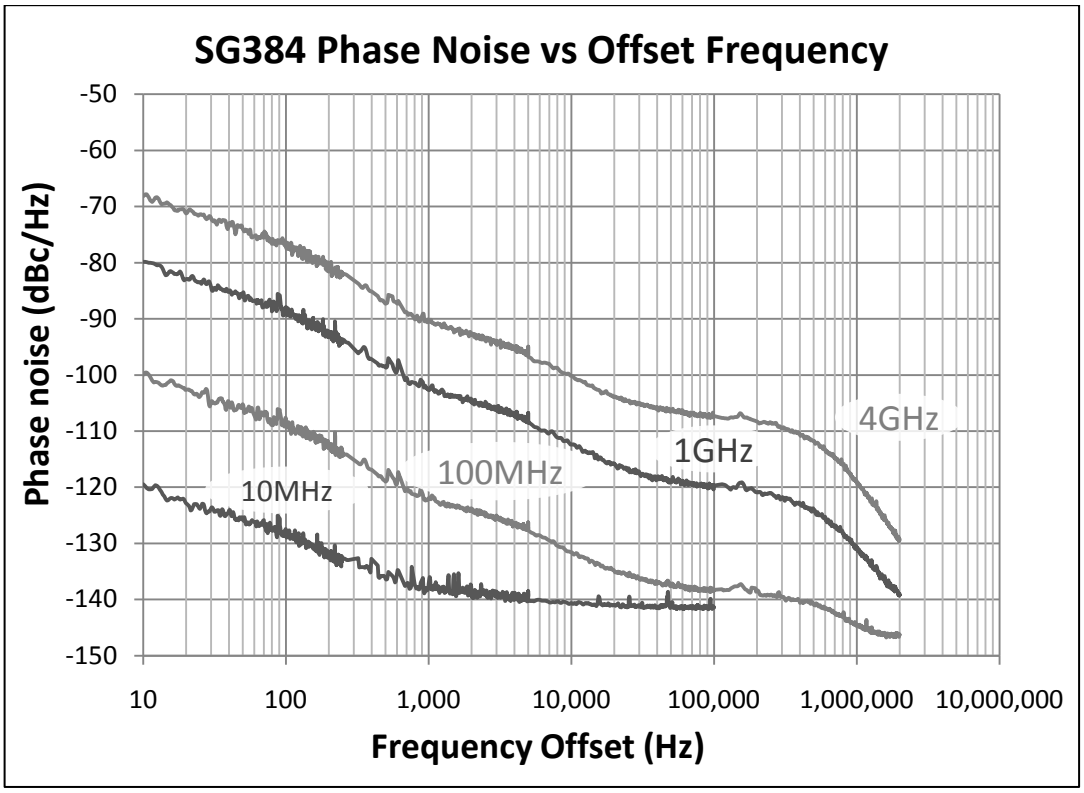
Output	Rear-panel SMA
Voltage range	±10 V
Offset voltage	<20 mV
DC accuracy	±0.2 %
DC resolution	5 mV
Output resistance	50 Ω
Current limit	20 mA

Computer Interfaces (all are standard)

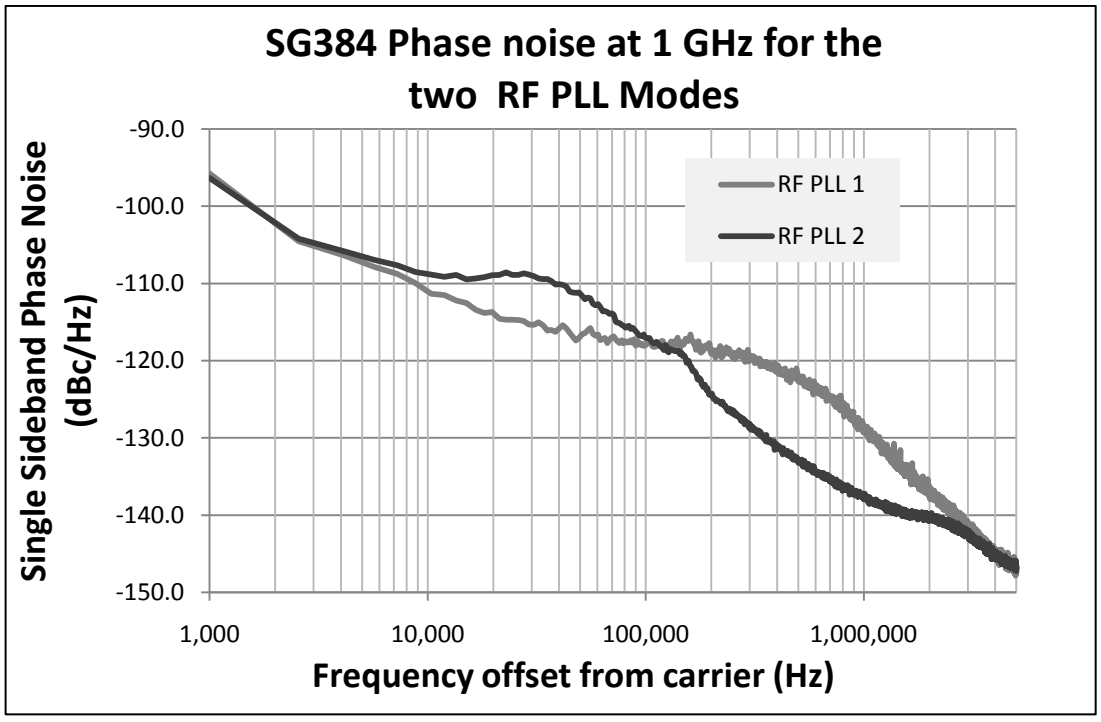
Ethernet (LAN)	10/100 Base-T. TCP/IP & DHCP default.
GPIB	IEEE-488.2
RS-232	4.8k-115.2k baud, RTS/CTS flow

General

Line power	<90 W, 90 to 264 V_{AC}, 47 to 63 Hz with PFC
EMI Compliance	FCC Part 15 (Class B), CISPR-22 (Class B)
Dimensions	8.5” × 3.5” × 13” (W × H × D)
Weight	<10 lbs
Warranty	One year on parts and labor



Graph 2: Single Sideband Phase Noise



Graph 3: Single Sideband Phase Noise for RF PLL Modes

Quick Start Instructions

Step by Step Example

With the power button in the Standby position, connect the SG384 to a grounded outlet using the power cord provided.

(1) On the SG384

(a) Push in the POWER button to turn on the unit.

(b) Load default settings by pressing the key sequence : [SHIFT] [0] [Hz % dBm]

(2) On the oscilloscope

(a) Set channel 1 for 200 mV / division, 50 Ω input termination

(b) Set the time scale to 100 ns / division

(c) Connect the SG384 BNC output to the oscilloscope channel 1

(d) Set the trigger for AC, rising edge, channel 1 and adjust threshold as necessary

(i) There should be a sine wave with ten cycles shown of 630 mV_{PP} (corresponding to 1 mW into 50 Ω or 0 dBm).

(3) On the SG384

(a) Press the [FREQ] key

(i) Press the SELECT ◁ key three times to select the 1 MHz digit.

(ii) Press the ▽ key five times to change the frequency to 5 MHz

(iii) The display should now have five cycles shown.

(b) Press key sequence [2] [MHz]

(i) The oscilloscope should show two cycles of a sine wave.

(4) On the SG384

(a) Press [AMPL] repeatedly until the 'BNC' menu is displayed

(i) Press key sequence [+/–][6][dBm]

(b) The oscilloscope will now have a sine wave of 315 mV_{PP}

Refer to the detailed instructions that follow for more information on the operation of the SG384.

Introduction

Feature Overview

The SG384 Signal Generator is a high precision DC to 4 GHz (8 GHz with installation of option 2) synthesizer. The advance modulation capabilities, bandwidth, and precision of the SG384 make it an ideal instrument for many applications. The intuitive and efficient front panel allows direct entry of parameters.

The SG384 builds upon three generations of instruments at SRS:

1) The DS3xx series of DDS based Synthesized Function Generator — provides a conceptual base for certain aspects of the SG384 – offering rich modulation sources and DDS based waveform generation, precision RF outputs, as well as an established and widely accepted user interface.
2) The CG635 Synthesized Clock Generator provides a basis for the synthesis architecture utilized in the SG384, allowing a very high degree of frequency precision while simultaneously providing low phase noise and spurious content.
3) Finally, the DG645 Digital Delay Generator provided a base platform of software, microprocessor, and Field Programmable Gate Arrays — allowing the SG384 to implement real-time instrument functions that can be dynamically modified to meet complex requirements for the different operating modes in a time and cost efficient manner. The SG384 is also built upon a proven and tested software, firmware, and user interface model.

Various new technologies have also been leveraged to realize the SG384 — some of these include very high frequency DDS chips (≥ 1 GHz), larger FPGAs supporting DSP operations, and utilization of RF components that are cost effective and technically mature.

One area involves a novel new approach to Direct Digital Synthesis called Rational Approximation Synthesis (please see the appendix on page 168 for a detailed explanation).

All of these taken together allow the realization of the high performance, cost competitive, and functionally rich SG384 Synthesizer operating from DC to 8 GHz.

The SG384's front panel provides two separate outputs. A Type-N connector provides frequencies from 950 kHz to 4.05 GHz with powers (amplitudes) of –110 to +13 dBm (0.707 μV_{RMS} to 1 V_{RMS}). The BNC connector provides frequencies from 1 µHz to 62.5 MHz with powers (amplitudes) from –47 to +13 dBm (1 mV_{RMS} to 1 V_{RMS}). Both the Type-N and BNC allow for output typical powers (amplitudes) of up to 16.5 dBm (1.5 V_{RMS}) at relaxed signal specifications.

The SG384's user interface allows direct access to all of the main synthesizer functions, with lesser used functions assigned to secondary (or shifted) keys.

The rear panel provides additional functionality including an input for an external 10 MHz timebase, a modulation interface, and various optional interfaces, including outputs that extend the operation up to 8.10 GHz. GPIB, RS-232, and Ethernet are standard.

The SG384 may be operated as a single tone CW synthesizer for crystal clear frequency generation. For a 1 GHz output the SG384 has –75 dBc of SFDR and a single sideband phase noise of less than −116 dBc / Hz at 20 kHz offset from carrier. The SG384 has a frequency resolution of 1 µHz with accuracies of 0.002 ppm using the standard OCXO. With an optional rubidium timebase the accuracy is increased to 0.0001 ppm.

The standard SG384 also supports a wide range of modulation functions — AM, FM, ΦM, Pulse, and Noise. The technology utilized allows for broad modulation deviations and rates with very low distortion products. Option 3 allows I/Q modulation.

The SG384 supports frequency sweeps for the characterization of networks and other analysis. The sweep spans are frequency dependent. For frequencies greater than 62.5 MHz, sweep spans are set on octave boundaries (62.5 to 125 MHz, 125 to 250 MHz, etc.). For frequencies below 62.5 MHz, sweeps can span the entire range (DC to 62.5 MHz). The SG384 allows sweep rates up to 120 Hz, with saw tooth, triangle, or sin sweeps supported.

The rear panel has a frequency doubler option to extend the frequency operating range to 8.1 GHz with powers (amplitudes) from –10 to +13 dBm (70.7 mV_{RMS} to 1.0 V_{RMS}).

The rear panel also supports optional differential clock outputs. These operate over frequencies from 1µHz to 4.05 GHz. They replicate the synthesized frequency with edge transitions of less than 35 ps, programmable amplitude of 0.4 to 1 V_{PP}, and offsets of ±2 V_{DC}.

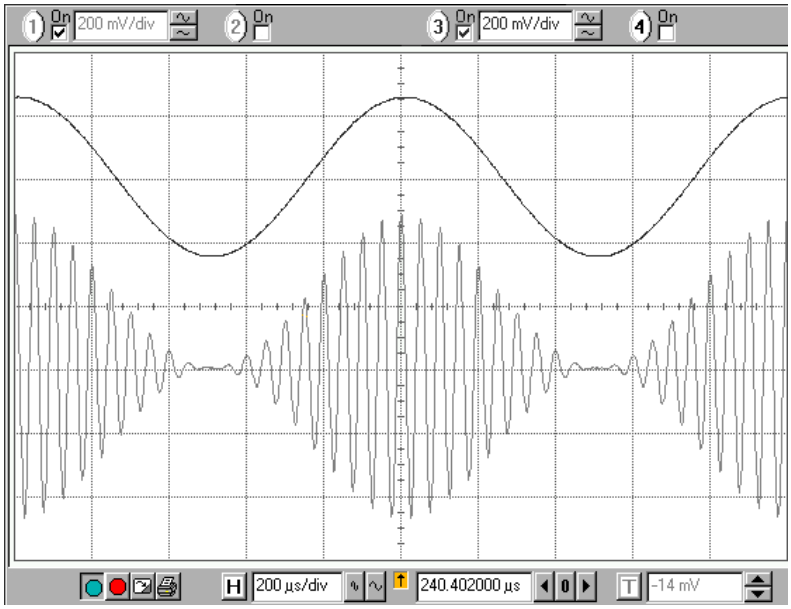
Waveform Overview

The following waveforms and spectral plots demonstrate some of the SG384's capabilities:

Waveform 1 is a 20 kHz carrier being amplitude modulated by a 1 kHz sine wave. The top trace is the rear panel Modulation output, while the bottom trace is the front-panel BNC output:

Set the SG384 as follows:

Frequency	20 kHz
Amplitude BNC	1 V_{PP}
Offset BNC	0 V
Modulation	
Type	AM
Function	Sine
Rate	1 kHz
Depth	100%
ON	

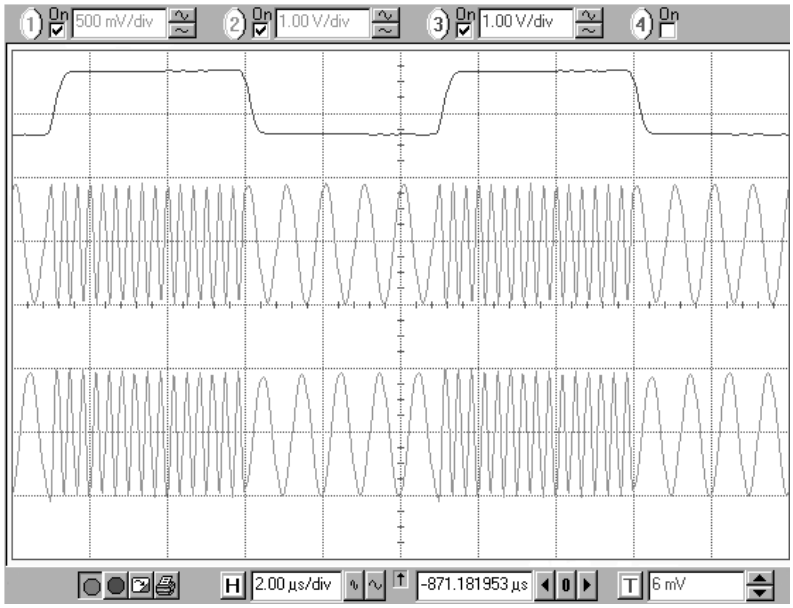


Waveform 1: AM Modulation

In Waveform 2, the internal modulator is set to FM between 1 MHz and 3 MHz with a 100 kHz square wave. The top trace is the real panel Modulation output, while the middle and bottom traces are the front panel BNC and N-Type outputs.

Set the SG384 as follows:

Frequency	2 MHz
Amplitude	
BNC	1 V_{PP}
N-Type	2 V_{PP}
Modulation	
Type	FM
Function	Square
Rate	100 kHz
Deviation	1 MHz
On	

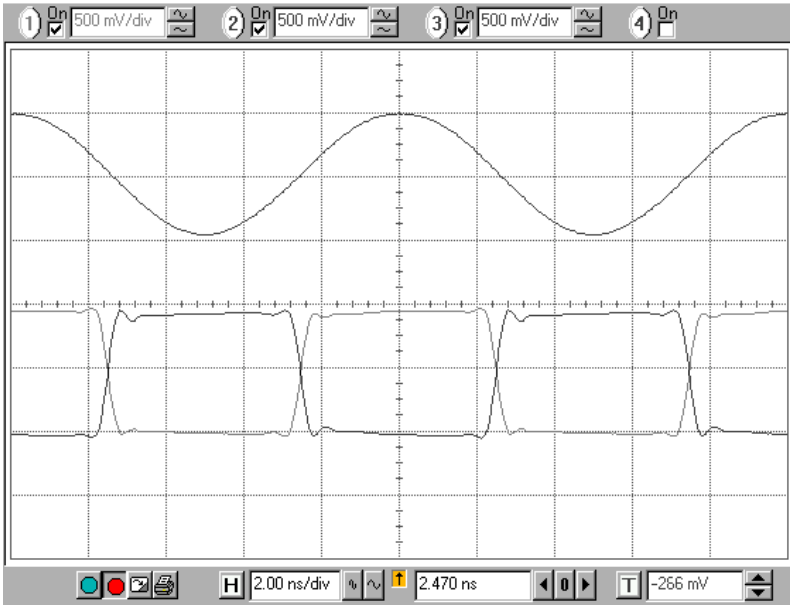


Waveform 2: FSK Modulation

Waveform 3 shows the optional rear panel clock outputs with the frequency set to 100 MHz. The top trace is front panel N-Type output with the differential clock outputs depicted by the lower traces. The displayed transition times are limited by the 1.5 GHz bandwidth of the oscilloscope.

Set the SG384 as follows:

Frequency	100 MHz
Amplitude	
N-Type	1 V_{PP}
Clock	1 V_{PP}
Offset Clock	0 V
Modulation	Off

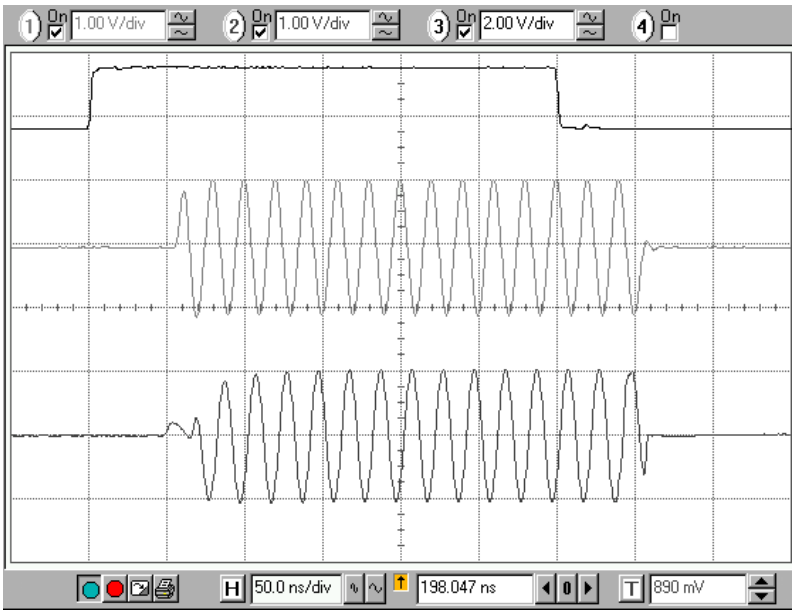


Waveform 3: Clock Outputs

Waveform 4 is a 50 MHz carrier being pulse modulated with a 1 MHz, 300 ns pulse waveform. The upper trace is the timing signal with the middle trace being the BNC output, and the lower trace being the RF output. There are delays of 50 ns in the gating circuitry as shown.

Set the SG384 as follows:

Frequency	50 MHz
Amplitude	
N-Type	2 V_{PP}
BNC	2 V_{PP}
Modulation	
Type	Pulse
Function	Square
Period	1 µs
Duty Factor	30%
ON	



Waveform 4: Pulse Modulated Output

Spectral Overview

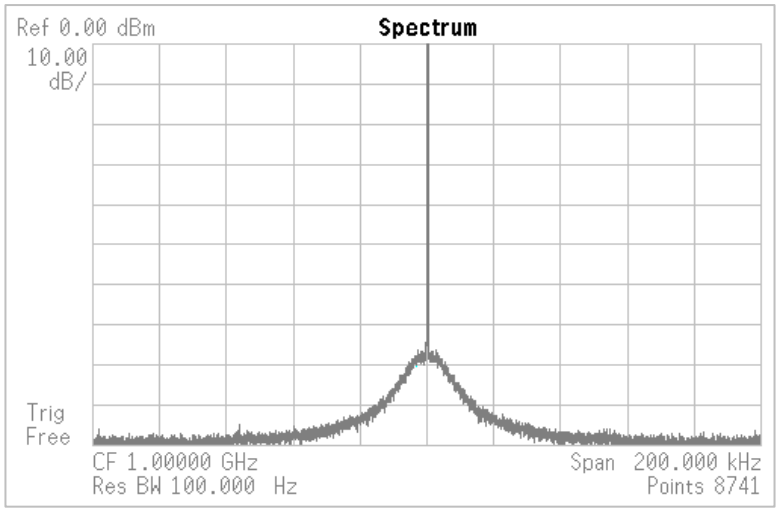
Waveform 5 shows a direct measurement taken on a spectrum analyzer with a 200 kHz span and 100 Hz RBW. The noise floor of the spectrum analyzer dominates over most of the 200 kHz span.

Set the SG384 as follows:

Frequency	1 GHz
Amplitude N-Type	0 dBm
Modulation	OFF

Spectrum Analyzer set for:

Center Frequency	1 GHz
Span	200 kHz
Resolution BW	100 Hz



Waveform 5: Unmodulated 1 GHz Output

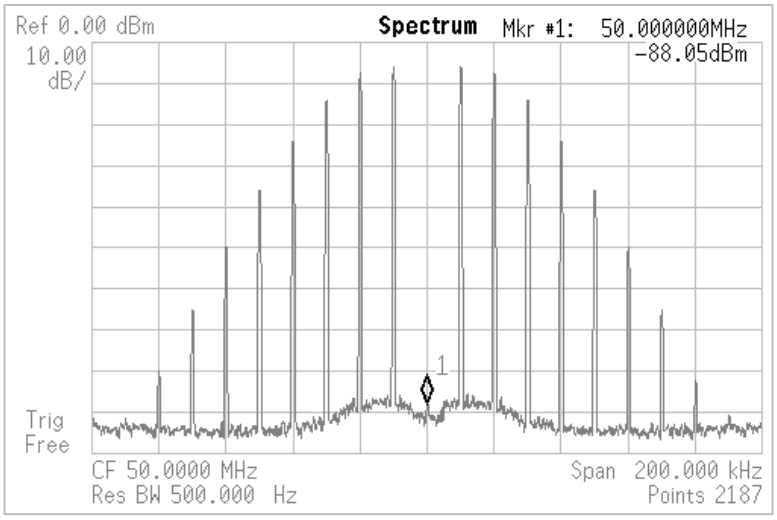
Waveform 6 depicts a 50 MHz carrier frequency modulated at a rate of 10 kHz and a deviation of 24.0477 kHz, for a modulation index β = 2.40477. The carrier amplitude is proportional to the Bessel function $J_0(\beta)$ and has its first zero at 2.40477, and thus suppresses the carrier.

Set the SG384 as follows:

Frequency	50 MHz
Amplitude N-Type	0 dBm
Amplitude BNC	0 dBm
Modulation	
Type	FM
Function	Sine
Rate	10 kHz
Dev	24.04 kHz
ON	

Spectrum Analyzer set for:

Center Frequency	50 MHz
Span	200 kHz
Resolution BW	500 Hz



Waveform 6: 50 MHz with FM Carrier Suppressed

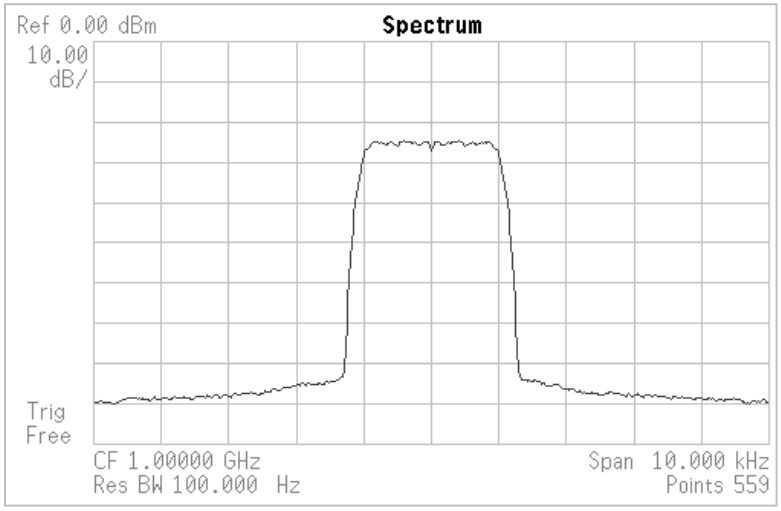
Option 3 allows I/Q modulation for output frequencies from 400 MHz to 4.05 GHz. Two signal sources may be used for modulation: the external I & Q inputs or an internal noise generator. The external I & Q inputs are on the rear panel. The internal noise generator has adjustable noise bandwidth from 1 Hz to 50 kHz. Waveform 7 is a 1 GHz carrier being modulated by the internal noise generator with 1 kHz noise bandwidth.

Set the SG384 as follows:

Frequency	1 GHz
Amplitude	
N-Type	–10 dBm
Modulation	
Type	I/Q
Function	Noise
Dev (ENBW)	1.0 kHz
ON	

Spectrum Analyzer set for:

Center Frequency	1 GHz
Span	10 kHz
Resolution BW	100 Hz



Waveform 7: I/Q Modulation using internal noise source

An unmodulated carrier at the analyzer's reference frequency (1 GHz in this case) appears as a single dot in the I/Q plane. When the carrier frequency is offset, the single dot moves in a circle about the center of the I/Q plane. The pattern shown occurs when the carrier amplitude is modulated with 100 % depth at a rate of five times the carrier offset frequency (creating five lobes). The symmetry of the lobes indicates that there is no residual phase distortion (AM to ΦM conversion) in the amplitude modulator. The narrow line of the trajectory is indicative of low phase and amplitude noise.

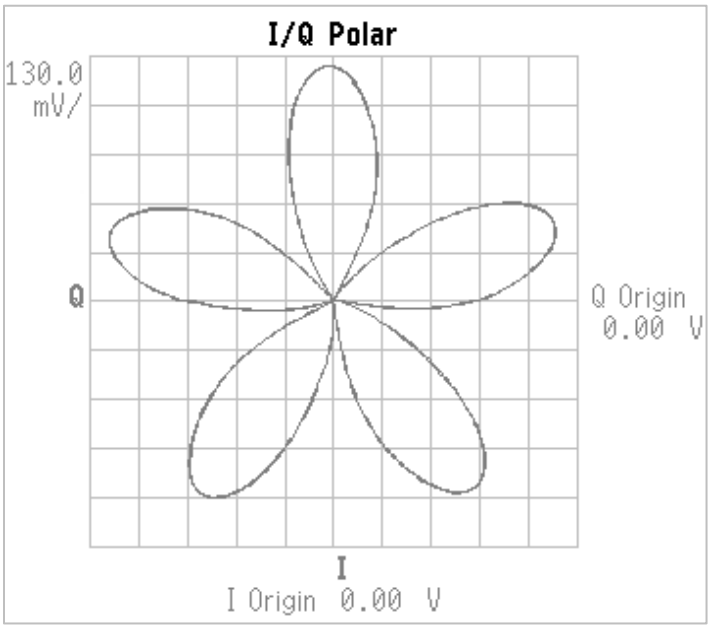
Set the SG384 as follows:

Frequency	1.000001 GHz
Amplitude	
N-Type	0 dBm
Modulation	
Type	AM
Function	Sine
Rate	5.0 kHz
Depth	100 %
ON	

Spectrum Analyzer set for:

Center Frequency	1 GHz
Span	10 kHz
Resolution BW	100 Hz

NOTE: Connect the SG384's Timebase output to the Spectrum Analyzer's external reference input.



Waveform 8: I/Q Polar Plot of 1 GHz Referenced to 1.000001 GHz AM of 5 kHz at 100 %

Front-Panel Overview

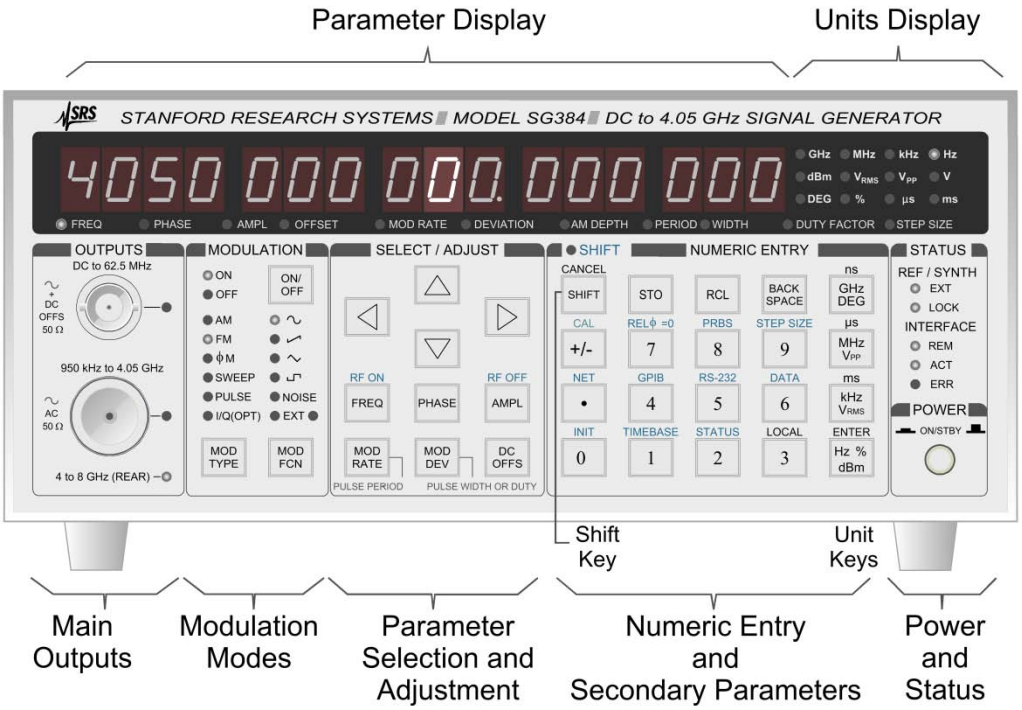


Figure 1: The SG384 Front Panel

The power switch is located in the lower right corner of the front panel. Pushing the switch enables power to the instrument. Pushing the switch again places the instrument in stand-by mode, where power is enabled only to the internal timebase.

The front panel is divided into seven sections (or "Panes"): Parameter Display, Units Display, OUTPUTS, MODULATION, SELECT/ADJUST, NUMERIC ENTRY, and STATUS.

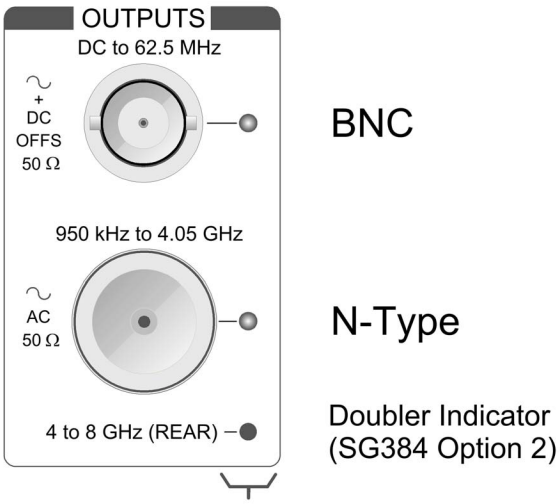
Parameter and Units Display

The SG384 has a sixteen digit display showing the value of the currently displayed parameter. The LEDs below the display indicate which parameter is being viewed. Error messages may also appear in the display, briefly.

The Units Display highlights the units associated with a parameter. Note that a given parameter may have multiple views. For example, the RF output amplitude may be viewed in units of dBm, V_{RMS}, or V_{PP}.

Main Output

These are the synthesizer's main signal outputs. Two types of connectors are provided due to the bandwidths covered by the instrument.



BNC Output

Signals on this connector are active for frequency settings between DC and 62.5 MHz. The amplitude may be set independently for levels from 1 mV_{RMS} to 1 V_{RMS} (–47 dBm to 13 dBm). Increase amplitude setting of 1.5 V_{RMS} (16.5 dBm) are allowed with relaxed signal specifications. Additionally, the BNC output may be offset by $\pm$ 1.5 V_{DC}.

NOTE: The BNC output is protected against externally applied voltages of up to $\pm$ 5 V.

N-Type Output

Signals on this connector are active for frequency settings between 950 kHz and 4.05 GHz. The amplitude may be set independently for levels from −110 dBm to 13 dBm (0.7 μV_{RMS} to 1 V_{RMS}). Increase amplitude settings of 16.5 dBm (1.5 V_{RMS}) are allowed with relaxed signal specifications.

NOTE: The N-type output is protected against externally applied voltages of up to 30 V_{DC} and RF powers up to +25 dBm.

Indicators

Three LEDs are used to indicate which of the outputs are active: BNC, N-Type, and the 4 to 8 GHz (REAR) Doubler.

The Doubler LED is lit only when Option 2 is installed and when the frequency is greater than 4.05 GHz.

Modulation Modes

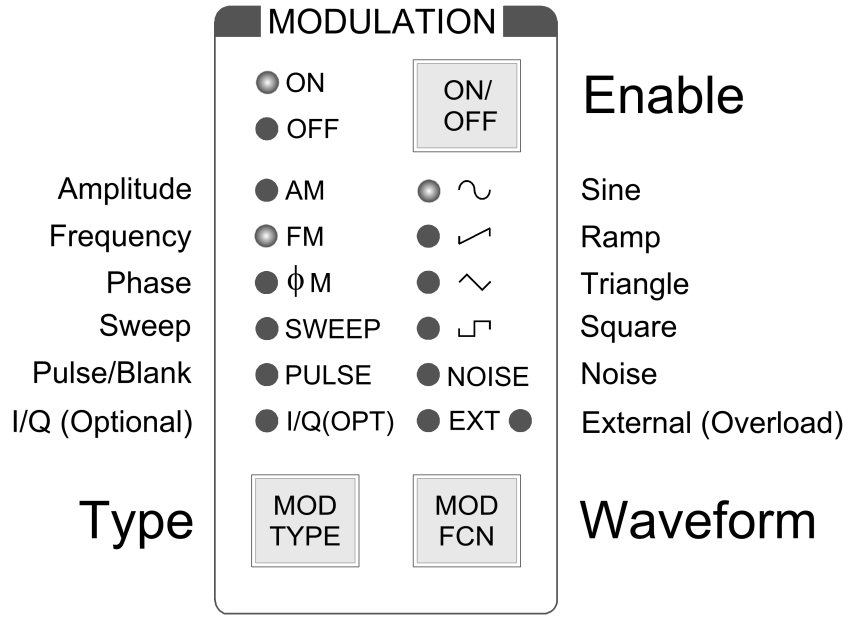
The Modulation pane displays the present modulation state and enables the user to control both the type and function of the modulation.

The [ON/OFF] key enables modulation.

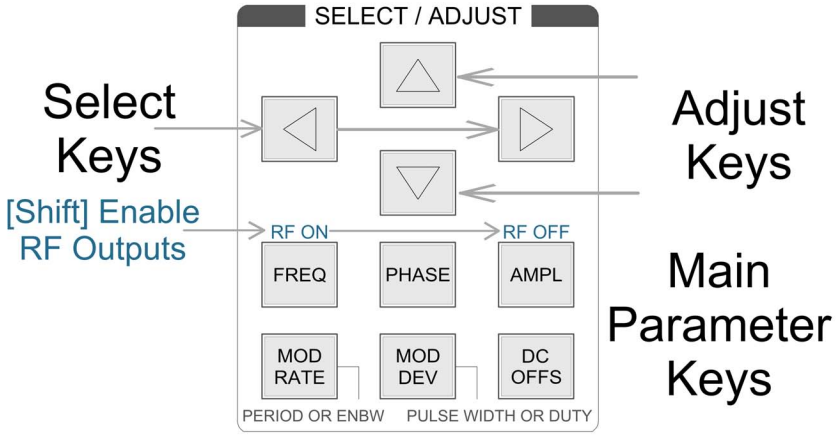
The [MOD TYPE] key allows selection of the type of modulation (via the ADJUST △ and ▽ keys). The types of modulation available are AM, FM, ΦM, Sweep, and Pulse. IQ modulation is available as an option.

The [MOD FCN] key allows the selection of the modulation waveform (via the ADJUST △ and ▽ keys). The available waveforms include sine, ramp, triangle, square wave, and noise.

The rear panel external modulation input can also be used in either for AM, FM, ΦM or Pulse. When the external source is selected, the signal level is monitored. If the external source exceeds operational limits the overload LED turns on and remains on until the condition is removed.



Parameter Selection and Adjustment



Display Navigation

The SELECT/ADJUST section determines which main parameter is shown on the front panel display. The six basic displays for viewing and modifying instrument settings are shown in Table 1. Each display is activated by pressing the correspondingly labeled key.

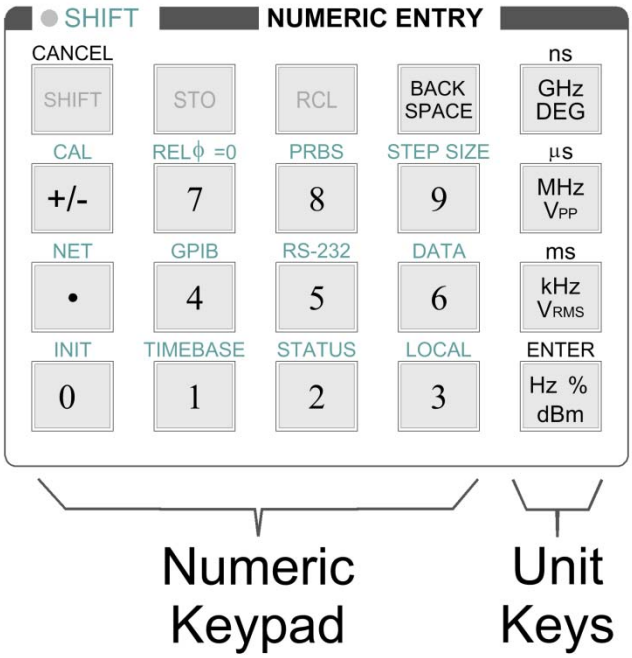
Table 1: SG384 Main Parameter Keys

Label	Value Shown in Main Display When Pressed
FREQ	Current Frequency (f_c)
PHASE	Current Phase
AMPL	Current Amplitude – sequences through outputs
DC OFFS	Current Offset – sequences through the outputs
MOD RATE	Current Modulation Rate (Pulse Period or ENBW)
MOD DEV	Current Modulation Deviation (Pulse Width or Duty)

For Parameter menus with multiple items, repeatedly pressing the Parameter key allows cycling through all of its parameters. For example, in the default configuration multiple key presses of the [AMPL] key will cycle through the various available outputs BNC, Clock, and N-Type.

Some of the parameters will have a blinking digit (the cursor). The cursor indicates which digit will be modified when the ADJUST △ and ▽ keys are pressed. The SELECT ◁ and ▷ keys allow adjusting the cursor for the desired resolution (the step size may also us the shifted function to allow numeric entry).

Numeric Entry and Secondary Parameters



This pane is used for changing the currently displayed numeric parameter directly. A parameter is entered numerically and completed by pressing any of the unit keys. Corrections can be made using the BACK SPACE or the entire entry may be aborted by pressing the CANCEL key.

For example, to set the frequency to 1.0001 GHz, press the [FREQ] key followed by the key sequence of [1] [•] [0] [0] [0] [1] [GHz].

This pane also allows access to secondary (or "Shifted") functions. The secondary functions are listed above the key in light blue text. A secondary function is accessed by first pressing the SHIFT key (indicated by the SHIFT LED being on) followed by pressing the desired secondary function key.

For example, to set the incremental value for frequency to 12 kHz press [FREQ] [SHIFT] [STEP SIZE], followed by the sequence [1] [2] [kHz].

Numeric or SHIFT entries may be aborted at any time by pressing the CANCEL key.

Stepping Up and Down

Most instrument settings can be stepped up or down by a programmed amount. The blinking digit identifies the current cursor position and step size. The cursor shows the digit that will change if the parameter is incremented or decremented via the ADJUST keys. Pressing the ADJUST △ (▽) key causes the displayed parameter to increment (decrement).

Step Size

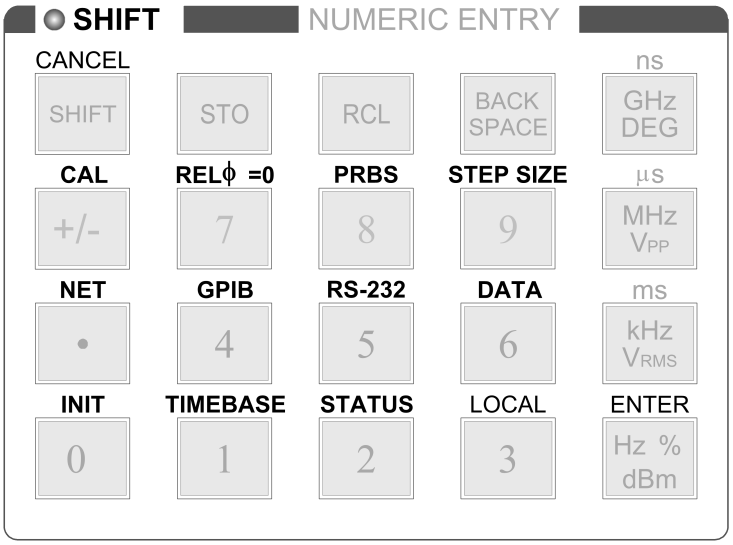
Pressing the ADJUST △ and ▽ keys increments or decrements the value of the selected digit on the numeric display (to change the selected digit use the SELECT ◁ and ▷ keys). To view the step size use the SHIFT [9] (STEP SIZE).

The step size can be changed using the numeric keypad followed by the appropriate unit. To set the step size to an arbitrary value use the SHIFT [9] the enter the desired step size followed by the appropriate unit type. For example, to change the frequency's step size to 1.25 MHz, first press [Shift] then [9] followed by 1.25 and finally the [MHz] unit key. When the cursor is changed to another digit (using the SELECT ◁ or ▷ keys) the step size returns to its default value.

Store and Recall Settings

The [STO] and [RCL] keys are for storing and recalling instrument settings, respectively. Instrument settings include modulation configuration and all associated step sizes. Up to nine different instrument settings may be stored in the locations 1 to 9. To save the current settings to location 5, press the keys [STO], [5], [ENTER], sequentially. To recall instrument settings from location 5, press the keys [RCL], [5], [ENTER] sequentially. Note: the INIT key is used to recall default instrument settings. See Default Factory Settings in the Operations chapter on page 52 for a list of default settings.

Secondary Functions



Many of the keys in the MODIFY section have secondary functions associated with them. The secondary functions are listed above the keys. The [5] key, for example, has RS-232 above it. The meaning of the secondary functions is summarized in Table 2.

Table 2: Secondary Functions

Label	Primary Key	Function Description
CAL	+/-	Adjust the timebase, and selects the PLL filter mode
REL Φ =0	7	Defines the current phase to be 0 degrees and displays phase
PRBS	8	Allows access to the length of the Pseudo-Random Binary Sequence generator
STEP SIZE	9	Set the incremental value used by the ADJUST keys
NET	•	Configure the Ethernet interface
GPIB	4	Configure the GPIB interface
RS-232	5	Configure the RS-232 interface
DATA	6	Display the most recent data received over any of the remote interfaces
INIT	0	Load default instrument settings
TIMEBASE	1	Displays the installed timebase and its status
STATUS	2	View TCP/IP (Ethernet), error, or instrument status, as well as running Self-Test
LOCAL	3	Go to local. Enables front panel keys if in remote mode.

A more detailed description of each of the secondary functions is given in the Secondary Functions section of the Operation chapter (page 45).

The secondary functions can only be accessed when the shift mode is active, which is indicated by SHIFT LED in the main display. The SHIFT mode can be toggled on and

off by pressing the [SHIFT] key. For example, to configure the PRBS length, press [SHIFT] [8] to access the PRBS secondary function.

For menu items with multi-parameter settings, the SELECT ◁ and ▷ keys allow selection of the various menu items. The MODIFY △ and ▽ keys may be used to modify a parameter. For example, the first option in the NET menu is TCPIP ENABLE/DISABLE. Use the MODIFY △ and ▽ keys to change the setting as desired. Then press SELECT ▷ to move to the next option which is DHCP ENABLE/DISABLE. Continue pressing the SELECT ▷ until all TCPIP settings have been configured as desired.

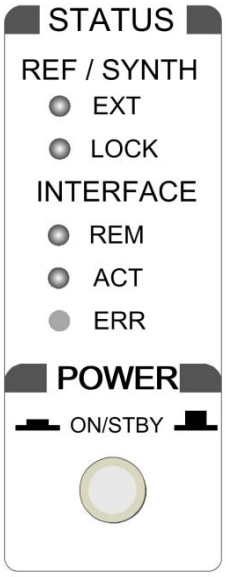
Cancel

The [SHIFT] key also functions as a general purpose CANCEL key. Any numeric entry, which has not been completed, can be canceled by pressing the [SHIFT] key. Because of the dual role played by the SHIFT key, the user may have to press [SHIFT] twice to reactivate SHIFT mode. The first key press cancels the current action, and the second key press re-activates SHIFT mode.

Power and Status

The Power and Status pane encompass the power switch and displays the status of the timebase and remote interface(s):

Status Indicators



REF / SYNTH

In the upper right portion of the front panel are two groups of LED indicators. The upper group is labeled REF / SYNTH and indicates the status of the internal timebase. The EXT LED indicates that the SG384 has detected an external 10 MHz reference at the timebase input BNC on the rear panel. If detected, the SG384 will attempt to lock its internal clock to the external reference.

The LOCK LED indicates that SG384 has locked its internal frequency synthesizer at the requested frequency. Normally this LED will only extinguish momentarily when the frequency changes or an external timebase is first applied to the rear input. If the LED stays off, it indicates that the SG384 may be unable to lock to the external timebase. This is most commonly caused by the external frequency being offset by more than 2 ppm from 10 MHz.

INTERFACE

The lower group of LED indicators is labeled INTERFACE. These LEDs indicate the current status of any active remote programming interface (Ethernet, RS-232, or GPIB).

The REM LED turns on when the SG384 is placed in remote mode by one of the remote interfaces. In this mode, all the front panel keys are disabled and the instrument can only be controlled via the remote interface. The user can return to normal, local mode by pressing the [3] key (also labeled [LOCAL]). The ACT LED flashes when a character is received or sent over one of the interfaces. This is helpful when troubleshooting communication problems. If a command received over the remote interface fails to execute due to either a parsing error or an execution error, the ERR LED will turn on. Information about the error is available in the STATUS secondary display.

POWER

The power switch has two positions: STANDBY (switch out) and ON (switch in).

In STANDBY mode, power is only supplied to the internal timebase and the power consumption will not exceed 25 watts.

In ON mode, power is supplied to all circuitry but the power consumption will not exceed 90 watts.

Rear-Panel Overview

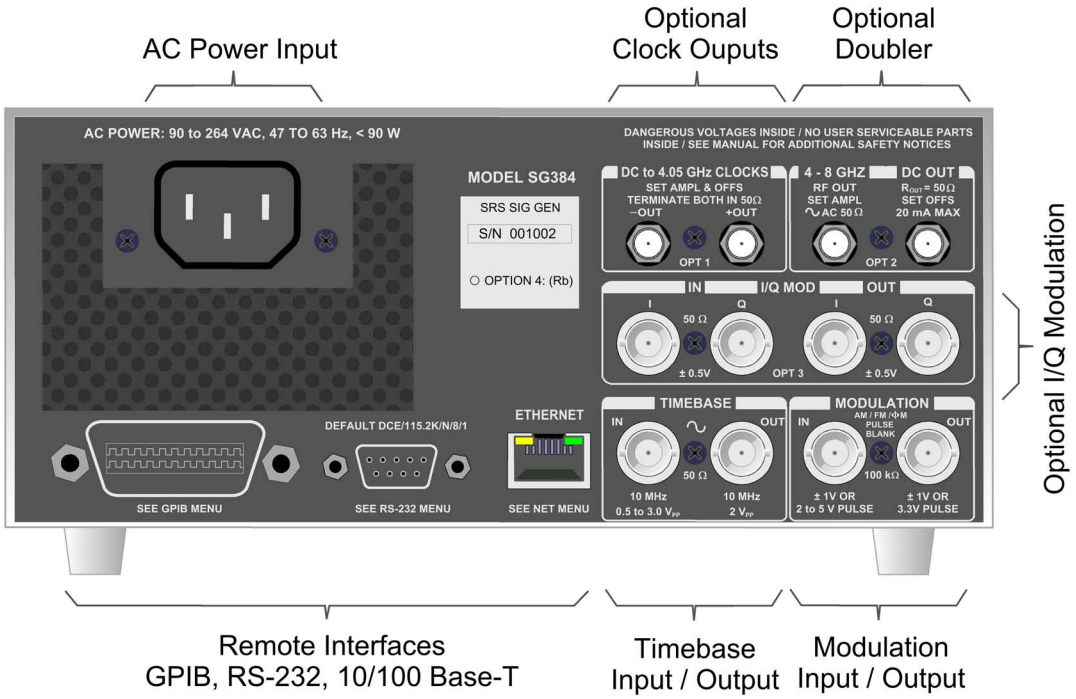


Figure 2: The SG384 Rear Panel

The rear panel provides connectors for AC power, remote computer interfaces, external frequency references, and various additional options.

AC Power

Connect the SG384 to a power source through the power cord provided with the instrument. The center pin is connected to the SG384 chassis so that the entire box is earth grounded.

The SG384 will operate with an AC input from 90 to 264 V, and with a frequency of 47 to 63 Hz. The SG384 requires 90W and implements power factor correction.

Connect the SG384 to a properly grounded outlet. Consult an electrician if necessary.

Timebase

10 MHz IN

This input accepts an external 10 MHz reference. The external reference should be accurate to at least 2 ppm, and provide a signal of no less than 0.5 V_{PP} while driving a 50 Ω impedance. The SG384 automatically detects the presence of an external reference, asserting the front panel EXT LED, and locking to it if possible. If the SG384 is unable to lock to the reference, the LOCK LED is turned off.

10 MHz OUT

The SG384 also provides a 10 MHz output for referencing other instrumentation to the SG384's high stability OCXO or optional Rubidium Timebase.

Remote Interfaces

The SG384 supports remote control via GPIB, RS-232, or Ethernet. A computer interfaced to the SG384 can perform any operation that is accessible from the front panel. Programming the SG384 is discussed in the Remote Programming chapter on page 55.

Before attempting to communicate with the SG384 over the target interface, please refer to the respective Remote Programming Configuration section on page 55.

GPIB

The SG384 comes standard with a GPIB (IEEE-488) communications port for communications over a GPIB bus. The SG384 supports the IEEE-488.1 (1978) interface standard. It also supports the required common commands of the IEEE-488.2 (1987) standard.

RS-232

The RS-232 port uses a standard 9 pin, female, subminiature-D connector. It is configured as a DCE and supports baud rates from 4.8 kb/s to 115 kb/s. The remaining communication parameters are fixed at 8 Data bits, 1 Stop bit, No Parity, with RTS/CTS configured to support Hardware Flow Control.

Ethernet

The Ethernet uses a standard RJ-45 connector to connect to a local area network (LAN) using standard Category-5 or Category-6 cable. It supports both 10 and 100 Base-T Ethernet connection and a variety of TCP/IP configuration methods.

Modulation

IN

External modulation is applied to this input. The input impedance is 100 kΩ with a selectable input coupling of either DC or AC (4 Hz roll off).

For analog modulations (AM, FM, ΦM), a signal of ±1 V will produce a full scale modulation of the output (depth for AM or deviation for FM and ΦM). It supports bandwidths of 100 kHz and introduces distortions of less than –50 dB.

For Pulse/Blank modulation types, this input is used as a discriminator that has a fixed threshold of +1 V.

OUT

This output replicates the modulation waveform and has a 50 Ω reverse termination. When using the internal source for AM, FM, and ΦM, it provides a waveform determined by the function and rate settings with an amplitude of ±1 V_{PP} into a high impedance. During external analog modulation, this output mirrors the modulation input.

For Pulse modulation, the output is a 3.3V logic waveform that coincides with the gate signal.

Rear-Panel Optional Outputs

Three rear panel options are available on the SG384: a high speed clock outputs, a frequency doubler for extending the SG384's frequency output to 8.1 GHz, and IQ modulator inputs for the N-Type output.

Option 1: Clock Outputs

The clock outputs provide a digital representation of the synthesized signal for frequencies up to 4.05 GHz on a pair of SMA type connectors. The outputs are differential signals with transition times of 35 ps (20 % to 80 %). They are commonly adjustable for amplitudes from 0.40 to 1.00 V, offsets of ± 2 V, with a resolution of 5 mV.

For frequencies above 62.5 MHz, the jitter on the clock signals will be less than 300 fs with a measurement bandwidth of 5 kHz to 5 MHz. For frequencies below 62.5 MHz the rms jitter will be less than 0.01 % × U.I (Unit Interval).

Option 2: 8 GHz Frequency Doubler

This option extends the frequency range of the SG384 to 8.1 GHz with power levels of up to 16.5 dBm. A DC output port is available for providing biasing of external circuits. Both of these signals use SMA type connectors.

RF OUT

This output is operational for frequencies from 4.05 to 8.1 GHz. This output is AC coupled and is adjustable over a range of –10 to +16.5 dBm. The RF output supports FM, ΦM, and Swept modulation.

DC OUT

This output provides DC voltage which is settable over a ± 10 V range with 5 mV of resolution.

Option 3: I/Q Modulator

This option allows I/Q modulation on the front panel N-Type RF output for output frequencies between 400 MHz and 4.05 GHz.

Either an external source or the internal noise source may be selected.

I/Q IN

These inputs accept signals of ±0.5 V, corresponding to full scale modulation, and have 50 Ω input impedances. Both inputs support signal bandwidths from DC to 100 MHz.

I/Q OUT

These outputs duplicate the I/Q modulation waveforms (internally or externally).

All I/Q signals utilize BNC connectors located on the rear panel.

Operation

Introduction

The following sections describe the operation of the SG384. The first section describes the basics of setting the frequency, phase, amplitude, and offset. The second section explains sweeps and modulation. The third section explains storing and recalling setups and setting the computer interfaces.

The previous chapter described the function of the front panel keys based on their location on the front panel. This section provides guidelines for viewing and changing instrument parameters independent of their location on the front panel.

Power-On

At power on, the SG384 will briefly display “SG384” followed by the firmware version and the unit serial number. When power on initialization has completed, the SG384 will recall the last known instrument settings from nonvolatile memory.

The SG384 continuously monitors front panel key presses and will save the current instrument settings to nonvolatile memory after approximately five seconds of inactivity. To prevent the nonvolatile memory from wearing out, the SG384 will not automatically save instrument settings that change due to commands executed over the remote interface. The remote commands *SAV (*RCL) may be used to explicitly save (recall) instrument settings over the remote interface, if desired. See the SG384 Remote Programming section on page 55 for more information about these commands.

The SG384 can be forced to boot up to factory default settings. This is accomplished by power cycling the unit with the [BACK SPACE] depressed. All instrument settings, except for the remote interface configurations, will be set back to their default values. All calibration bytes will be reset to the values set at the factory at the time of shipment. See the Factory Default Settings section on page 52 for a list of default settings.

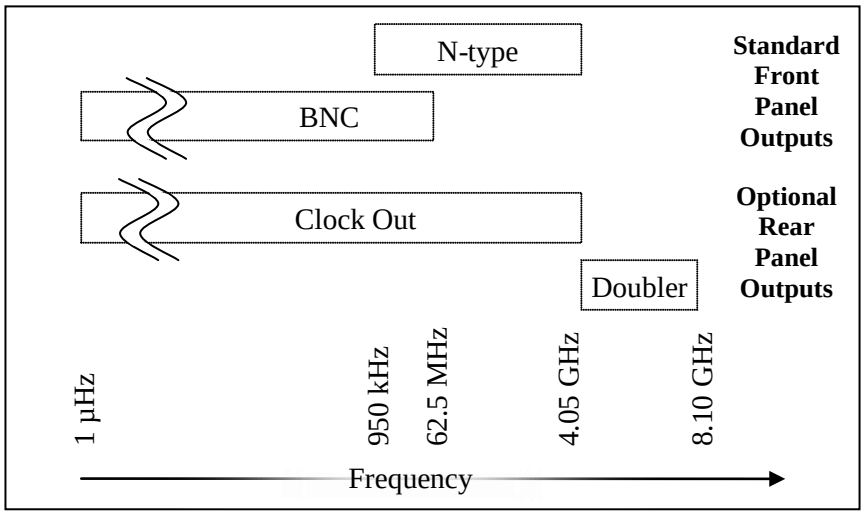
Synthesizer and Outputs

The SELECT/ADJUST pane allows access to the main parameters.

The SG384 operates over a wide range of frequencies. None of the four outputs (including the optional rear panel doubler and clock) operate across the entire frequency range. The associated parameters are inaccessible when the frequency is set outside of an output's operational range. As an example, if the frequency is set for 100 kHz, the N-type and Doubler (if installed) outputs are turned off, and their Amplitude parameters are not accessible.

Figure 3 indicates the operation of the outputs verses frequency. When the frequency is set outside the range of a given output, its associated parameters (Amplitude and Offset) become inaccessible.

Figure 3 - Outputs vs. Frequency



Setting Parameters

The SELECT/ADJUST section determines which parameter is shown in the main front panel display. The six keys for selecting the display of the main instrument settings are shown in Table 3. Each display is activated by pressing the corresponding labeled key.

Table 3: SG384 Main Display Parameters

Label	Value
FREQ	Current Frequency (f_c)
PHASE	Current Phase
AMPL	Current Amplitude – sequences through all outputs
DC OFFS	Current Offset – sequences through all outputs
MOD RATE	Current Modulation Rate (Pulse Period) and ENBW
MOD DEV	Current Modulation Deviation (Pulse Width or Duty Factor)

Frequency

Pressing [FREQ] displays the SG384's output frequency and turns on the FREQ LED.

The frequency may be entered in any of the standard units (GHz, MHz, kHz, or Hz). The current display may be normalized to a unit by pressing the desired unit key.

The frequency resolution is 1 µHz at all frequencies. The frequency setting determines which outputs may be active at any given time (see Figure 3 - Outputs vs. Frequency).

Phase

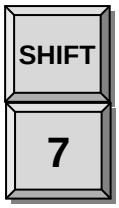
Pressing [PHASE] displays the SG384's phase and turns on the PHASE LED.

The phase is displayed in degrees and is adjustable over ± 360º. As the phase exceeds 360º, the parameter is normalized back to zero by setting the display to the new phase modulo 360º.

The phase resolution depends upon the current setting of the frequency. For the frequencies up to 100 MHz the phase resolution is 0.01°, with reduced resolution for higher frequencies. Table 4 shows the phase resolution verses frequency:

Table 4: Phase Resolution

Frequency Range	Phase Resolution
DC to 100 MHz	0.01°
100 MHz to 1 GHz	0.1°
1 GHz to 8.1 GHz	1.0°



In many situations it is useful to be able to normalize the present phase setting to zero. The SG384 allows this using the REL Φ=0 function ([SHIFT] [7] keys). This will set the phase parameter to zero, while preserving the current phase.

AMPL

Amplitude and Power

Pressing [AMPL] displays the SG384's output amplitude or power and turns on the AMPLITUDE LED.

The amplitude has a value for each of the installed outputs, and repeated pressing of [AMPL] sequences through all accessible parameters. Note however, that only those outputs that are active for the current frequency setting will be accessible.

All amplitudes (except for clock) may be displayed in units of dBm, V_{RMS}, or V_{PP}, with clock being restricted to V_{PP}. All stated values assume a load termination of 50 Ω.

Table 5 lists the range for the various units of the outputs:

Table 5: Output Power Range

		Calibrated Range Units			Uncal'ed Range(1)
		dBm	V_{RMS}	V_{PP}	
OUTPUT	N-type	–110 → +13	0.707µ → 1	2µ → 2.83	To 16.5 dBm
	BNC	–47 → +13	1.00m → 1	2.83m → 2.83	To 15.5 dBm
	Doubler	–10 → +13	0.0707 → 1	0.200 → 2.83	To 16.5 dBm
	Clock	N/A	N/A	0.4 → 1	N/A

If an output is set below its minimum value it will be disabled. This is indicated on the display as "off" and by extinguishing the associated output status LED.

(1) Note that the N-Type, BNC, and Doubler outputs support setting the power to an "uncal'ed" region. These output values are typical, and other specifications are not guaranteed for this region. Power levels of 16.5 dBm are achievable.

Figure for depicts the region for the N-Type output. The "uncal'ed" output power is reduced above 3.4 GHz to 14 dBm at 4 GHz.

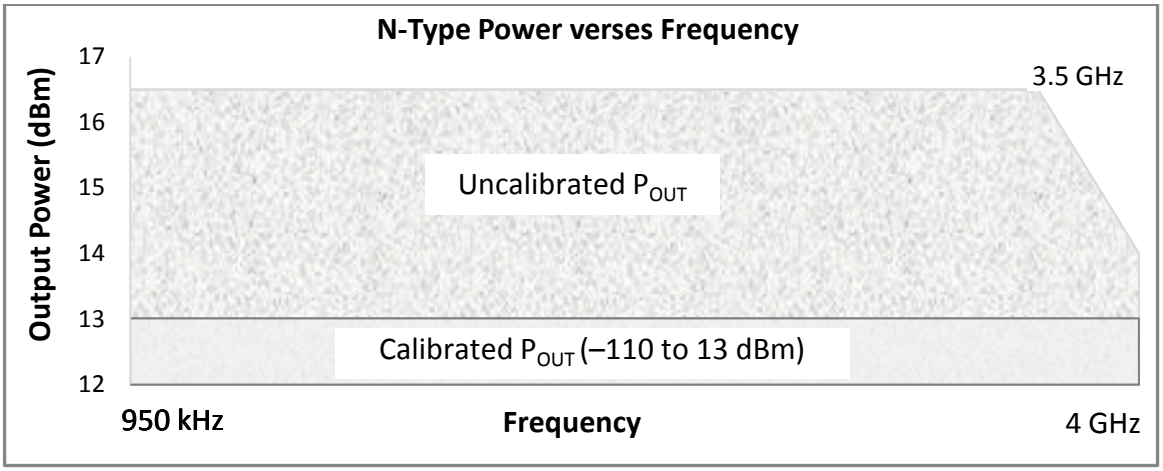


Figure 4: Uncal'ed N-Type Output Power

DC OFFS

DC Offset

Pressing [DC OFFS] displays the SG384's output offset and turns on DC OFFSET.

The DC offset has values for the BNC as well as some of the installed output options. Repeatedly pressing [DC OFFS] will sequence through all accessible parameters. For SG384's with the optional Doubler, the DC offset associated with the frequency doubler option is always accessible and active.

All DC offsets are displayed in V_{DC}. Table 6 gives the DC offset range for the various outputs:

Table 6: Offset Range

Output	DC Offset Range
N-type	N/A
BNC	±1.5V
Rear DC Offset	±10V
Clock	±2V

The BNC output will support offsets up to 1.5V. The BNC's maximum instantaneous voltage is limited to 1.9 V. Thus, the output provides 13 dBm (2.828 V_{PP}) at no offset, and is reduced linearly to 0 dBm (0.632 V_{PP}) for offsets of ±1.5 V. Figure 5 shows the relationship between BNC amplitude and offset settings.

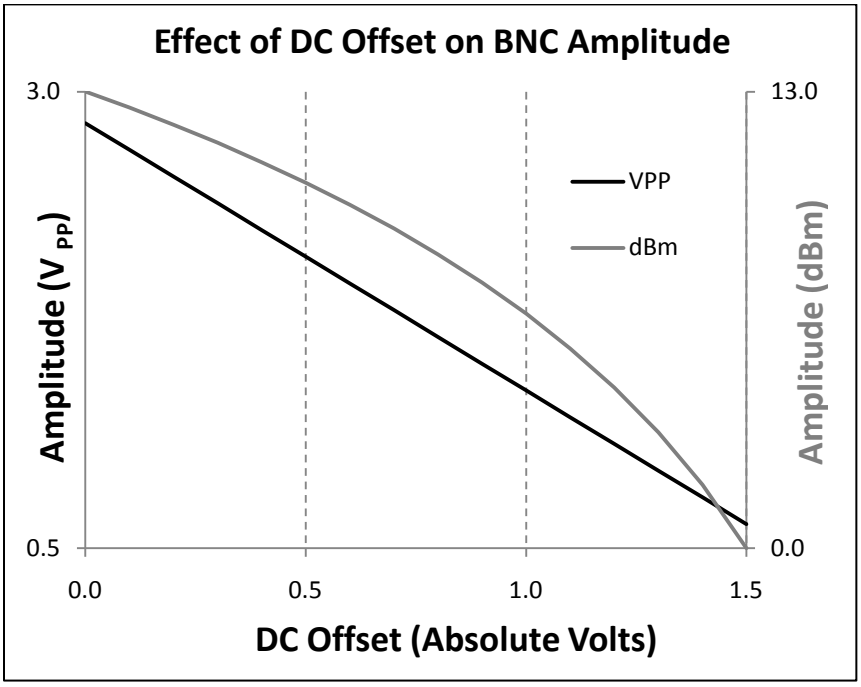


Figure 5: BNC Output vs. DC Offset

RF ON/RF OFF

These are shifted functions of the [FREQ]/[AMPL] keys, respectively.

When the [RF ON]/[RF OFF] are pressed there is a momentary display of "rf on" / "rf off", and the status LEDs for the outputs are set / cleared, respectively.

The [RF OFF] turns off all RF outputs, while setting the clock output to a static "off" state (+OUT to "low", –OUT to "high"). When an output is selected that is off the display will indicate the off status. For example, selecting the N-Type amplitude would display "ntype off".

The [RF ON] returns all RF outputs to their previously active levels.

Sweeps and Modulation

Introduction

This section describes the SG384's modulation capabilities. The SG384 has powerful and flexible built-in modulation functions, capable of AM, FM, ΦM, swept frequency, Pulse, and I/Q modulations. The modulation waveform may be a sine wave, square wave, ramp, triangle wave, noise, or external source. For additional flexibility the SG384 can also quickly cycle through a list of settings with an arbitrary combination of amplitude, frequency, phase, and modulation settings (see List Mode on page 83.)

Modulation Rate

The [MOD RATE] and [MOD DEV] keys are paired in operation and their parameters depend upon the current modulation type and function settings.

Pressing [MOD RATE] displays the SG384's modulation rate associated with the current modulation type and turns on either the MOD RATE (for AM/FM/PM and sweep) or the PERIOD (for pulse/blank) LEDs.

For the standard (AM/FM/ΦM) and sweep modulation types, this parameter is the frequency of the applied modulation waveform. The allowable range depends on both the type of modulation and the frequency selected.

For pulse modulation, this selects the period of the pulse. This is settable in 5ns increments from 1 µs to 10 s.

For I/Q noise modulation (option 3) this key sets the equivalent noise bandwidth (ENBW) of the modulation

Modulation Deviation

Pressing [MOD DEV] displays the deviation of the current modulation function. Depending on the modulation type, either the MOD DEV, AM DEPTH, WIDTH, or DUTY FACTOR is displayed.

During AM modulation, the AM depth is displayed and corresponds to the peak percentage that the output envelope will span. For example, if the amplitude is set to 1 V_{PP} and the depth is set for 50% the output envelope would span from 0.5 V to 1.5 V.

During FM and sweep modulations, the deviation corresponds to the peak frequency excursion applied to the carrier. For example, if the carrier is set to 1.1 MHz and the deviation is set to 0.1 MHz, the carrier will span between 1 MHz and 1.2 MHz.

During ΦM modulation, the deviation corresponds to the peak phase excursion applied to the carrier. For example, if the deviation is set to 10°, then the carrier will span ±10°.

During pulse/blank modulation, deviation allows the pulse width or duty factor to be changed. This parameter may be either a time ("t on" for pulse or "t_off" for blank) or a duty factor. For example, for a 1 µs pulse period, a width of 500 ns or a duty factor of 50% would be equivalent, and result in the output being on for 50% of the 1 µs period.

Modulation Pane

This determines which (if any) modulation will be applied to the outputs.

Modulation On/Off

The [ON/OFF] key toggles the modulation on/off and the current state is reflected by the ON/OFF LEDs.

Modulation Type

The [MOD TYPE] key allows the selection of which type of modulation will be applied to the synthesizer's output. The ADJUST △ ▽ keys are used to select the desired modulation type and the current selection is highlighted. The types of modulation available are AM, FM, ΦM, Sweep, and Pulse. Optional I/Q modulation is also available if option 3 is installed.

Modulation Function

The [MOD FCN] key selects one of the various functions to be applied. The ADJUST △ ▽ keys are used to select the desired modulation function. The current selection is highlighted.

For all modulation types (except I/Q) the rear panel external modulation source may be used. When installed, the I/Q modulation supports separate inputs for the I and Q signals.

Not all modulation types support all modulation functions. Table 7 shows which modulation types support which functions:

Table 7: Modulation Type vs. Function

Type \ Function	Sine	Ramp	Triangle	Square	Noise	External
AM / FM / ΦM	✓	✓	✓	✓	✓	✓
Sweep	✓	✓	✓			✓
Pulse				✓	✓	✓
I/Q (Optional)					✓	✓

Modulation Sources and Outputs

The SG384's modulation supports both internal and external sources. The modulating waveform is replicated on the rear panel Modulation output connector.

Linear Modulation

For AM / FM / ΦM, and Sweep, the modulation source can be either the internal generator or the rear panel external modulation input.

The internal modulation source is capable of generating sine, ramps, triangular, or square waves, at frequencies of up to 500 kHz. (The instrument limits the modulation rate to 50 kHz for output frequencies above 62.5 MHz.)

The rear panel external modulation input supports bandwidths of 500 kHz, but the modulation bandwidth is limited to 100 kHz for f_C greater than 62.5 MHz. The sensitivity is set such that a 1 V signal results in a full scale deviation (depth) in the output. For example: in ΦM, if the deviation is set for 10°, applying a level of –1 V produces a –10° shift; applying 0 V produces no shift; and applying +1 V produces a 10° shift.

When modulation is enabled using an internal source, the rear panel modulation output will provide a waveform of the selected function with a peak-to-peak amplitude of two volts. When external modulation is selected the modulation output tracks the applied signal.

Pulse Modulation

During pulse modulation, the internal source is a digital timing waveform that is settable from 1 µs to 10 s with 5 ns of adjustability. The parameters of the timing waveform are accessed via the [MOD RATE] and [MOD DEV] keys.

When an external input is selected the rear panel external modulation input is set for a threshold of 1V. The resulting signal is used in place of the internal source.

The modulation output is a 3.3 V logic signal, which tracks the pulse waveform.

Noise Modulation

All modulation types (except for sweep) support a form of noise modulation.

For linear modulation types, the noise source is pseudo random additive white Gaussian noise (AWGN). The bandwidth of the noise is set by the [MOD RATE] and the RMS deviation is set by the [MOD DEV].

A one-unit RMS deviation will result in roughly a five-unit peak deviation. This forces limits on the Noise Deviation corresponding to one fifth of their non-noise counterparts. For example, at a frequency of 500 MHz the maximum FM deviation for a sine wave function is limited to 4 MHz, and the noise deviation is limited to 800 kHz.

For linear modulation, the rear panel output will provide 200 mV_{RMS} that will be band limited to the selected modulation rate.

For pulse modulation, the noise source is a Pseudo Random Bit Sequence (PRBS). The bit period is set by the [MOD RATE]. The PRBS supports bit lengths of 2^n, for $5 \leq n \leq 19$ which correspond to a noise periodicity from 31 to 524287 periods. The bit length n is set via the [Shift] [PRBS] key.

During pulse PRBS modulation, the rear panel output will be a 3.3 V_{PP} waveform with a duty factor equal to $2^{n/2} / 2^{n-1}$ (approximately 50 %).

Internal Modulation Source

For linear modulations, the internal source can be viewed as a function generator (selected by the MOD FCN) that produces the desired waveform. The frequency is determined by the MOD RATE, and the amplitude is fixed at ± 1 V_{PP}.

For angular modulations (FM, ΦM, sweep), the synthesizer modulation sensitivity is set to the specified modulation deviation (frequency for FM and Sweep, degrees for ΦM).

For AM, the output attenuators are set to achieve the prescribed AM Depth with an input of +1 V.

For example, with the modulation type set for FM, and the deviation set for 1 kHz, the resulting output frequency will traverse ± 1 kHz about the SG384's frequency setting.

If, however, the modulation type is AM, and the depth is set for 50 %, the resulting waveform envelope will traverse ± 50 % about the SG384's amplitude setting.

Note that for the noise function the deviations are in RMS units, and the deviation limits are reduced to 1/5 of their non-noise counterparts.

Amplitude Modulation

The amplitude modulation can use either the internal modulation generator or an external source. The internal modulator can generate sine, ramp, triangle, square, or noise waveforms.

Amplitude modulation is not applied to the optional rear panel doubler output.

To select AM modulation, set the modulation type to AM and turn on the modulation.

Modulation Rate

Pressing [MOD RATE] displays the SG384's modulation rate and turns on the MOD RATE LED. The value may be set using the SELECT/ADJUST arrow keys or via a numeric entry and one of the [MHz] [kHz] or [Hz] unit keys.

The internal modulation support rates of 50 kHz for f_C above 62.5 MHz or 500 kHz for f_C less than or equal to 62.5 MHz. The Modulation rate supports 1 µHz of resolution at all frequencies.

External modulation supports bandwidths of 100 kHz.

Modulation Depth

Press [MOD DEV] to display and set the AM modulation depth, which also lights the AM DEPTH LED. The value may be set using the numeric entry and [%] unit keys, or using the SELECT/ADJUST arrow keys. This value has a range of zero to 100 % with a 0.1 % resolution.

A modulation depth of *X* percent will modulate the amplitudes by $\pm$ *X* percent. As an example, if the amplitude is set for 224 mV_{RMS} (0 dBm), with a modulation depth of 50%, the resulting envelope would traverse 112 to 336 mV_{RMS}.

NOTE: The outputs are limited to 1 V_{RMS} (+13 dBm). If the modulation is increased such that the peak envelope would exceed this limit, the SG384's amplitude will be automatically reduced, and the screen will momentarily display “output reduced”.

The following simulation plots demonstrate the time and frequency output for two amplitude modulation scenarios.

Figure 6 is a 1 kHz carrier modulated by a 100 Hz sine wave, and a modulation depth of 10 %. There are two sidebands offset by 100 Hz and each –26 dB from the carrier.

(Freq = 1000 Hz, Type = AM, Fnc = Sine, Mod Rate = 100 Hz, Mod Depth = 10 %)

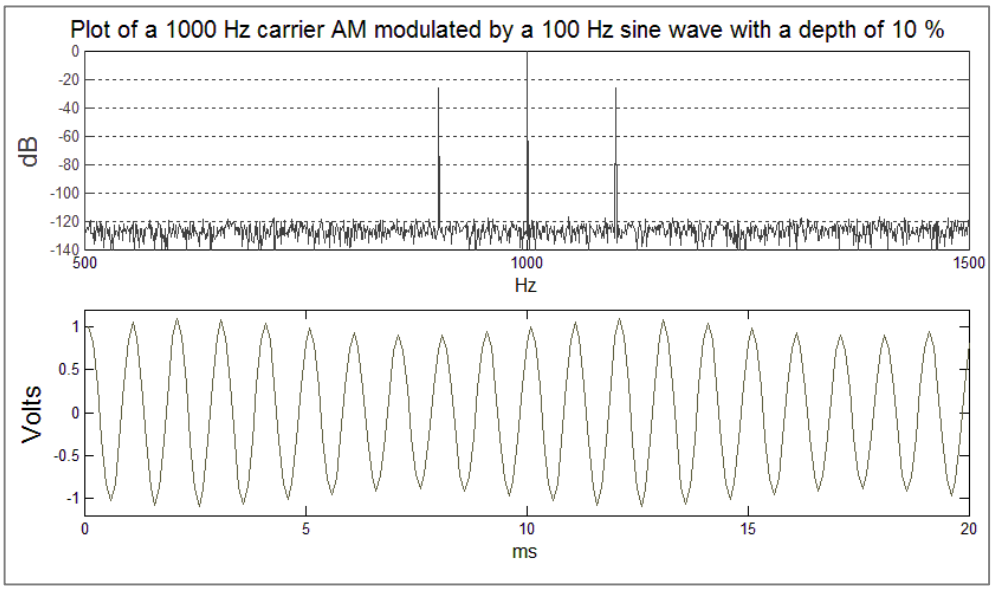


Figure 6: Simulation of AM

Figure 7 is of a 5 kHz carrier modulated by a 50 Hz square wave, with a modulation depth of 50 %. As can be seen the spectrum becomes much more complex.

(Freq = 5 kHz, Type = AM, Fnc = Squ. wave, Mod Rate = 50 Hz, Mod Depth = 50 %)

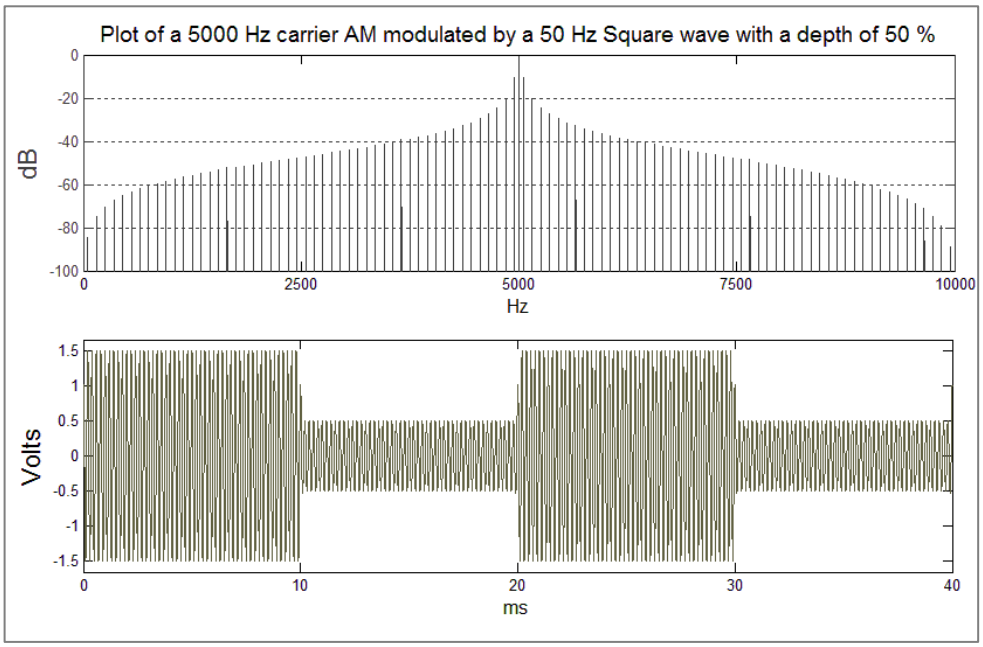


Figure 7: Simulation of AM

Frequency Modulation

The internal modulation generator or an external source may be used as the modulation source. The internal modulator can generate sine, ramp, triangle, square, or noise waveforms.

During FM, the output frequency traverses $f_C \pm$ deviation at the specified modulation rate. For example, if the frequency is set for 1000 MHz (1 GHz), and the modulation rate and deviation are set for 10 kHz and 1 MHz, respectively, then the output will traverse from 1000 MHz, up to 1001 MHz, down to 999 MHz, and back to 1000 MHz at a rate of 10 kHz (a period of 100 µs).

The optional rear panel doubler output can also be frequency modulated.

To select FM modulation, set the modulation type to FM and turn on the modulation.

The FM modulation parameters are dependent upon the frequency setting. Table 8 lists the FM parameters as a function of frequency. All frequency bands span octaves except for the first band. The internal FM rates correspond to the upper range that the internal function generator supports. The external bandwidth is defined as the SG384's −3 dB response referenced to the external modulation source. For the bands 2 to 8, the rates and bandwidths are similar. However, the deviation increases by a factor of two, from 1 to 64 MHz, for octaves 2 through 8.

The first band has unique FM capabilities in that it allows setting the deviation of the carrier frequency to the nearest band edge. If the carrier is set on the upper edge of 62.5 MHz, the deviation is allowed to be set to 1.5 MHz (5 % of f_C). This range also supports a wider internal rate and bandwidth of 500 kHz.

For example, if the frequency is set for 100 kHz, the deviation may be set from zero to 100 kHz.

Table 8: FM Modulation vs. frequency

Band	f_C Frequncy Range (band edges)	Internal FM Rates (1µHz to)	External FM BW (DC to)	FM Deviation (0.1 Hz to)
1	DC ⇒ 62.5 MHz	500 kHz	500 kHz	smaller of f_C or (64 MHz − f_C)
2	62.5 ⇒ 126.5625 MHz	50 kHz	100 kHz	2 MHz
3	126.5625 ⇒ 253.125 MHz			4 MHz
4	253.125 ⇒ 506.25 MHz			8 MHz
5	506.25 ⇒ 1012.5 MHz			16 MHz
6	1012.5 ⇒ 2025 MHz			32 MHz
7	2025 ⇒ 4050 MHz			64 MHz
8 (Option 2)	4050 ⇒ 8100 MHz			128 MHz

Modulation Rate

Pressing [MOD RATE] displays the SG384's modulation rate and turns on the MOD RATE LED. The value may be set using the SELECT/ADJUST arrow keys or via a numeric entry and one of the [MHz] [kHz] or [Hz] unit keys.

Internal modulation supports rates of 50 kHz for f_C above 62.5 MHz or 500 kHz for f_C less than or equal to 62.5 MHz, with 1 µHz of resolution.

External modulation supports bandwidths of 100 kHz.

Modulation Deviation

Press [MOD DEV] to display and set the FM deviation, which also turns on the DEVIATION LED. The value may be set using numeric entry and [MHz] [kHz] or [Hz] unit keys, or the SELECT / ADJUST arrow keys.

The deviation has a range that is dependent on carrier frequency band.

There are seven octaves above the lowest frequency range of DC to 62.5 MHz. The first octave (62.5 to 125 MHz) supports deviation of 1 MHz, with each succeeding octave doubling the deviation, thus achieving a 64 MHz of deviation at the 4 to 8 GHz octave (if the optional doubler is installed.)

NOTE: If the frequency is changed, the deviation may be adjusted as necessary to maintain limits imposed by the new frequency setting.

The following plots show two examples of FM modulation.

Figure 8 is the plot of a 1250 Hz carrier modulated by a 100 Hz sine wave with a deviation of 240.48 Hz. This is an interesting condition in that the carrier is almost totally suppressed.

(Freq = 1250 Hz, Type = FM, Fnc = Sine, Mod Rate = 100 Hz, Dev = 240.48 Hz)

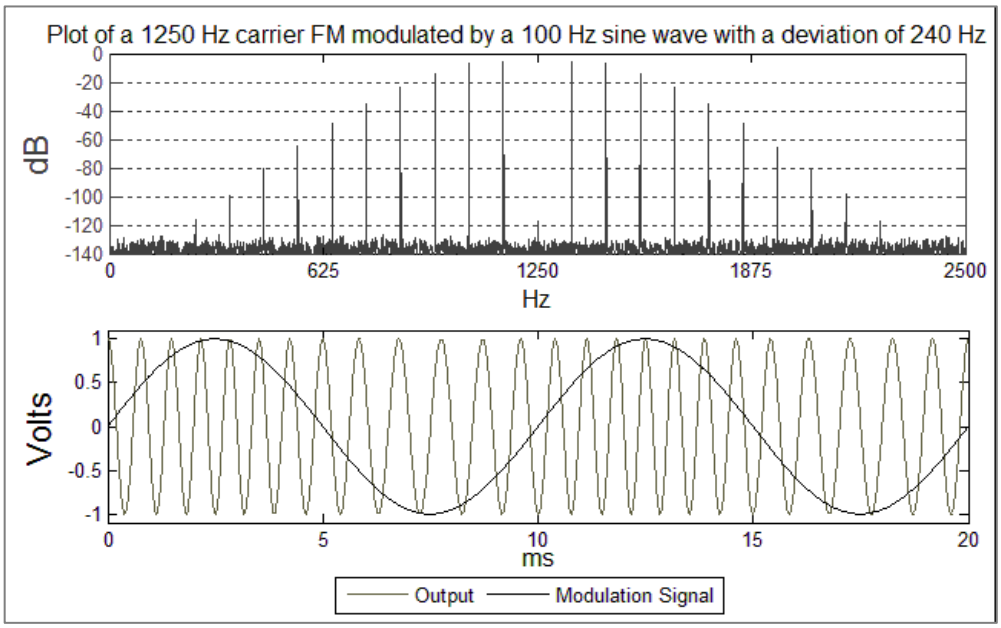


Figure 8: Simulation of FM

Figure 9 is of a 3000 Hz carrier modulated be a 100 Hz sine wave with a 1000 Hz deviation.

(Freq = 3000 Hz, Type = FM, Fnc = Sine, Mod Rate = 100 Hz, Dev = 1000 Hz)

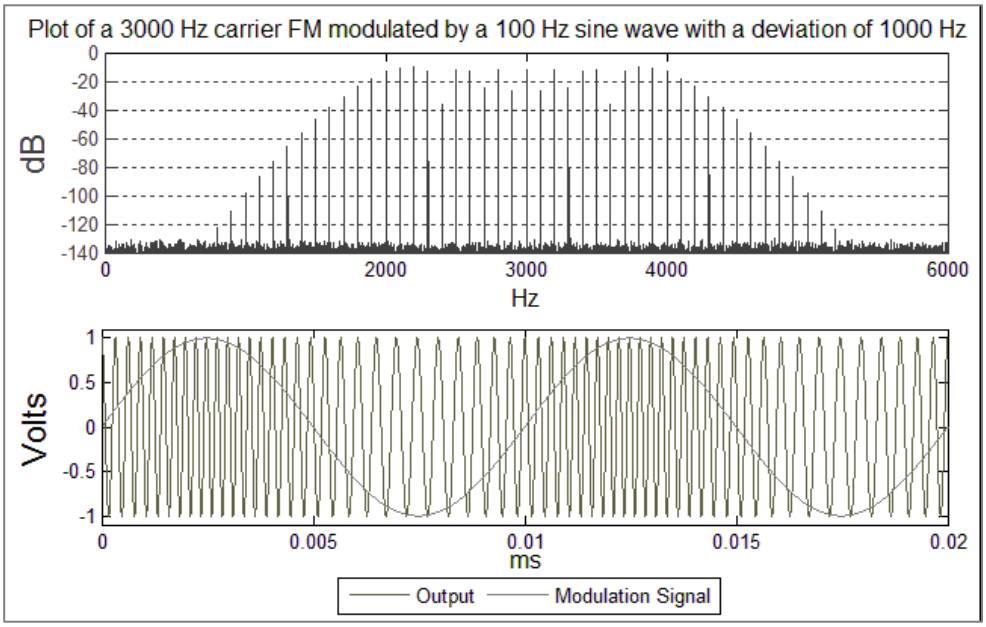


Figure 9: Simulation of FM

Phase Modulation

The phase modulation can use either the internal modulation generator or an external source. The internal modulator can generate sine, triangle, ramp, square, or noise waveforms.

The phase of the output traverses the specified deviation at the modulation rate. For example, with a frequency of 1000 MHz (1 GHz), and modulation rate and deviation set to 10 kHz and 45 degrees, respectively, the output will be a fixed frequency with its phase traversing ±45 degrees at a 10 kHz rate.

The optional rear panel doubler output can also be phase modulated.

To select phase modulation, set the Modulation type to ΦM and turn on Modulation.

Modulation Rate

Pressing [MOD RATE] displays the SG384's modulation rate and turns on the MOD RATE LED. The value may be set using the SELECT / ADJUST arrow keys or via a numeric entry and [MHz] [kHz] or [Hz] unit keys.

Modulation Deviation

Press [MOD DEV] to display and set the ΦM deviation, which turns on the DEVIATION LED. The value may be set using the numeric entry and the [DEG] unit key.

The phase resolution depends on the frequency setting. For frequencies below 100 MHz, the phase resolution is 0.01°. For frequencies between 100 MHz and 1 GHz the resolution is reduced to 0.1°, and is 1° for frequencies above 1 GHz.

For frequencies less than or equal to 62.5 MHz the accuracy of the phase deviation is 0.1 %. For frequencies above 62.5 MHz the accuracy is reduced to 3 %.

Figure 10 illustrates a 1250 Hz carrier modulated by a sine wave of 100 Hz with a modulation depth of 138°. This would result in a nearly suppressed carrier.

(Freq = 1250 Hz, Type = ΦM, Fnc = Sine, Mod Rate = 100 Hz, Dev = 137.8 Degrees)

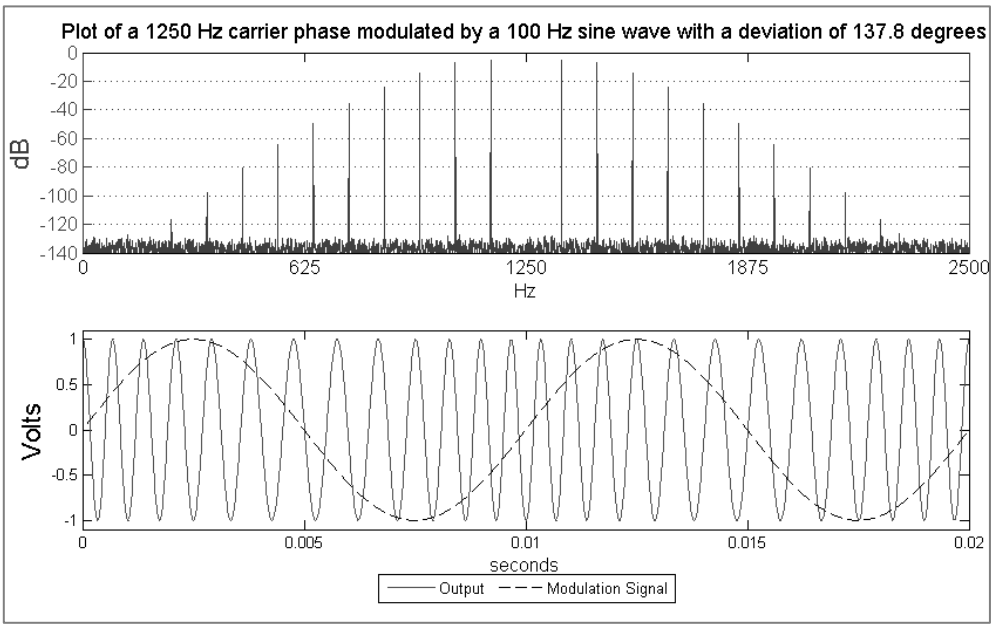


Figure 10: Simulation of ΦM

Figure 11 is of a 2 kHz carrier being modulated by a 100 Hz carrier at a deviation of 5.7°.

(Freq = 2000 Hz, Type = ΦM, Fnc = Sine, Mod Rate = 100 Hz, Dev = 5.7 Degrees)

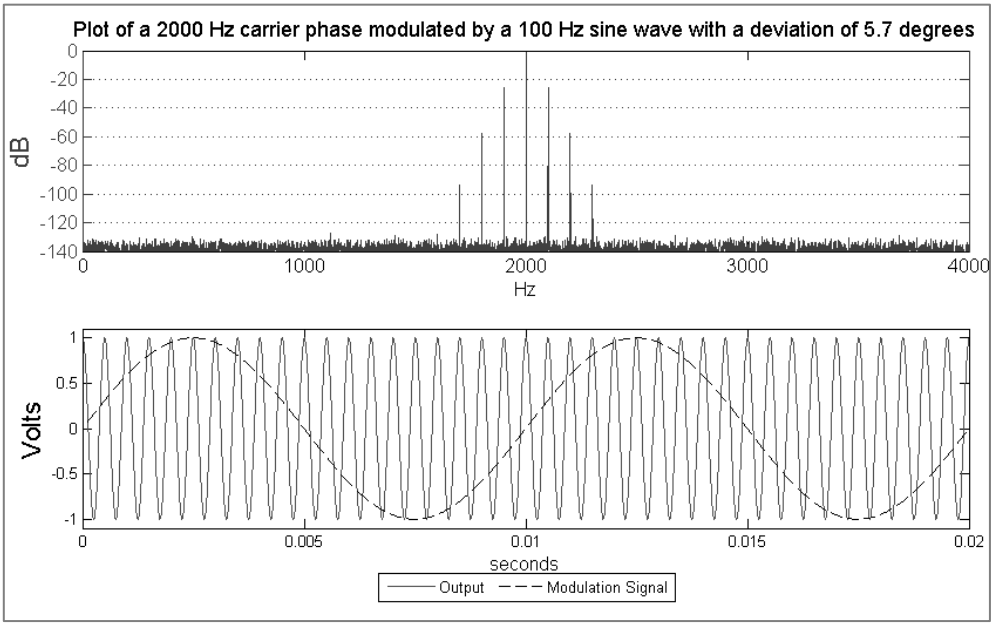


Figure 11: Simulation of ΦM

Pulse and Blank Modulation

Pulse modulation includes both pulse and blank modulation. Pulse and blank modulation are logical complements of each other – pulse modulation enables the output when the pulse waveform is "true", while blank modulation disables the output. The functions supported are square, noise Pseudo Random Binary Sequence (PRBS), and external.

For internal square wave function the SG384 has a 32-bit timing generator clocked by a 200 MHz source. This allows the period to be set from 1 µs to 10 s with a resolution of 5 ns. The pulse duration can then be set from 100 ns up to the period minus 100 ns.

For pulse (blank) modulation, the output is turned on (off) when the source is at logic "high".

Pulse modulation is not applied to the optional doubler output.

To select pulse modulation, set the modulation type to "pulse" and turn on modulation.

Pulse Period

Pressing [MOD RATE] displays the SG384's pulse modulation period and turns on the PERIOD LED. The value may be set using the SELECT/ADJUST arrow keys or via numeric entry plus one of the [ns] [µs] [ms] [enter] unit keys.

Pulse Width or Duty Factor

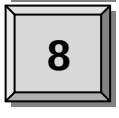
Press [MOD DEV] to display and set the pulse width, which also turns on either the WIDTH or DUTY FACTOR LED. The value may be set using numeric entry and [ns] [µs] [ms] [enter] or [%] unit keys, or the SELECT / ADJUST arrow keys.

PRBS Noise Modulation

When the noise function is selected, the SG384 replaces the pulse generator with a pseudo random binary sequence (PRBS) generator.

In this mode both the period as well as the bit length of the PRBS generator may be set.

The period is accessed via the [MOD RATE] key, and may set from 100 ns to 10 s, with 5 ns resolution.



The PRBS bit length may adjusted using the [Shift] [PBRS] key. The PRBS bit length may be set from 5 to 19 bits. The noise periodicity is variable from 31 to 524287 periods.

The resulting timing waveform is used to gate the N-Type and BNC outputs.

Figure 12 illustrates the output with a carrier of 10 kHz that is pulse modulated by a waveform with a 10 ms period and 10 % duty factor.

(Freq = 10k Hz, Type = Pulse, Fnc = Square, Mod Period = 10 ms, DF = 10 %)

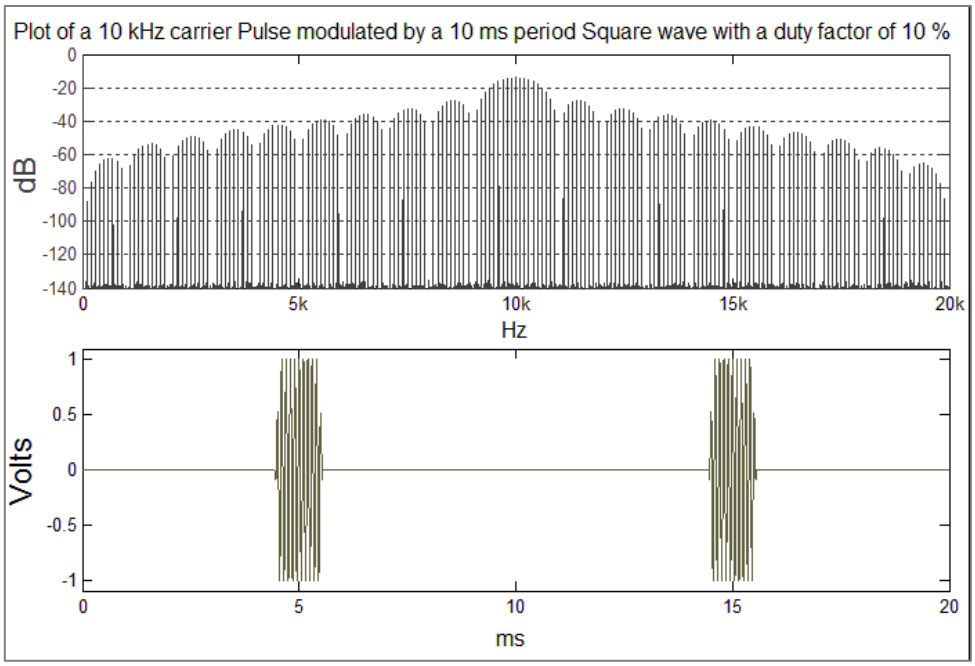


Figure 12: Simulation of Pulse modulation

Figure 13 illustrates a similar output, this time using blanking. A carrier of 10 kHz is blank modulated by a waveform with a 10 ms period and a 10 % duty factor.

(Freq = 10 kHz, Type = Pulse, Fnc = Square, Mod Period = 10 ms, DF = 10 %)

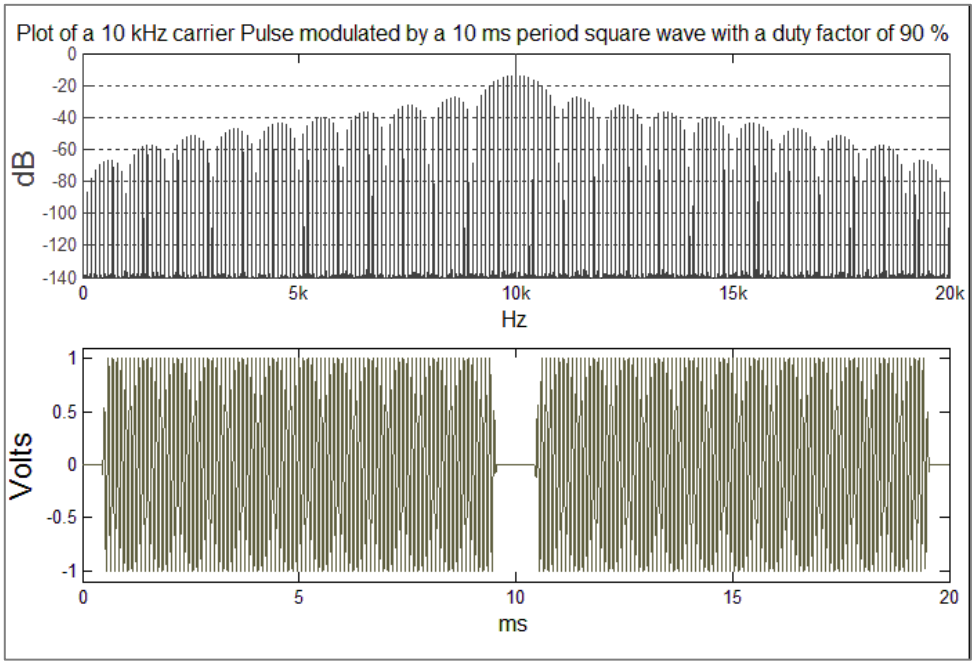


Figure 13: Simulation of Pulse modulation

Phase Continuous Frequency Sweeps

Frequency sweeps allow the traversing of an entire frequency band. The sweep modulation may use the internal sine, triangle, or ramp waveforms.

Sweep rates of up to 120 Hz and sweep ranges from 10 Hz up to an entire frequency band are supported with resolutions of 1 µHz.

The SG384 has eight frequency bands as shown in Table 9:

Table 9: Sweep Frequency Bands

Band	Frequency
1	DC ⇒ 62.5 MHz
2	59.375 ⇒ 128.125 MHz
3	118.75 ⇒ 256.25 MHz
4	237.5 ⇒ 512.5 MHz
5	475 ⇒ 1025 MHz
6	950 ⇒ 2050 MHz
7	1900 ⇒ 4100 MHz
8 (Option 2)	3800 ⇒ 8200 MHz

Frequency Sweep modulation can also be applied to the doubler output (optional).

To select Sweep modulation, set the Modulation type to “SWEEP” and turn on Modulation.

Sweep Rate

Pressing [MOD RATE] displays the SG384's modulation rate and turns on ‘MOD RATE’ LED. This value may be set using the SELECT/ADJUST arrow keys or via numeric entry plus one of the Hertz unit key.

The Rate may be set from 1 µHz to 120 Hz with a resolution of 1 µHz.

Sweep Deviation

Press [MOD DEV] to display and set to the Sweep deviation. This turns on the ‘DEVIATION’ LED. The value may be set using numeric entry plus one of the hertz unit keys, or the SELECT/ADJUST arrow keys.

The deviation may be set to sweep an entire band or any part.

Eexamples using the swept frequency modulation.

Figure 14 is a 2000 Hz carrier swept over 4000 Hz range (2000 Hz deviation) at a 100 Hz rate. This produces a sweep that spans from DC to 4000 Hz.

(Freq = 2000 Hz, Type = Sweep, Fnc = Saw tooth, Mod Rate = 100 Hz, Dev = 2000 Hz)

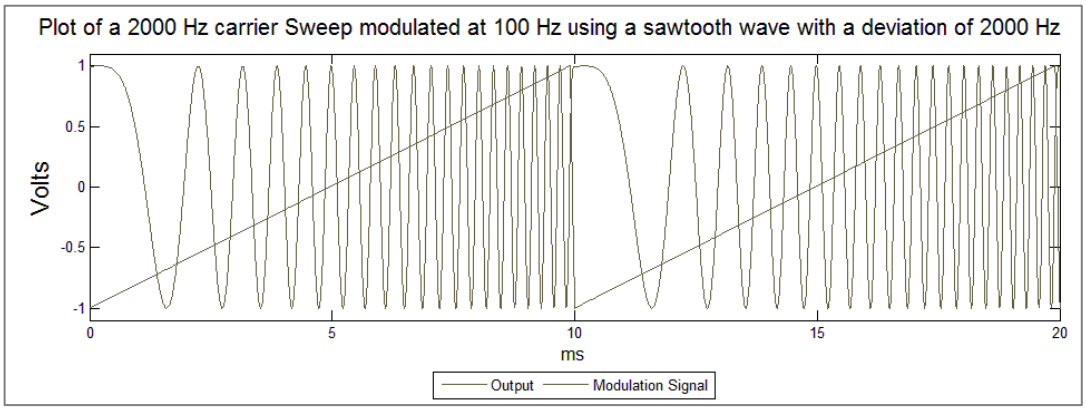


Figure 14: Simulation of Sweep modulation

Figure 15 is a 5000 Hz carrier swept at a 100 Hz rate with a 5000 Hz deviation. This produces a sweep that spans from DC to 10000 Hz.

(Freq = 5000, Mod Type = Sweep, Mod Fnc = Tri, Mod Rate = 100 Hz, Dev = 5000 Hz)

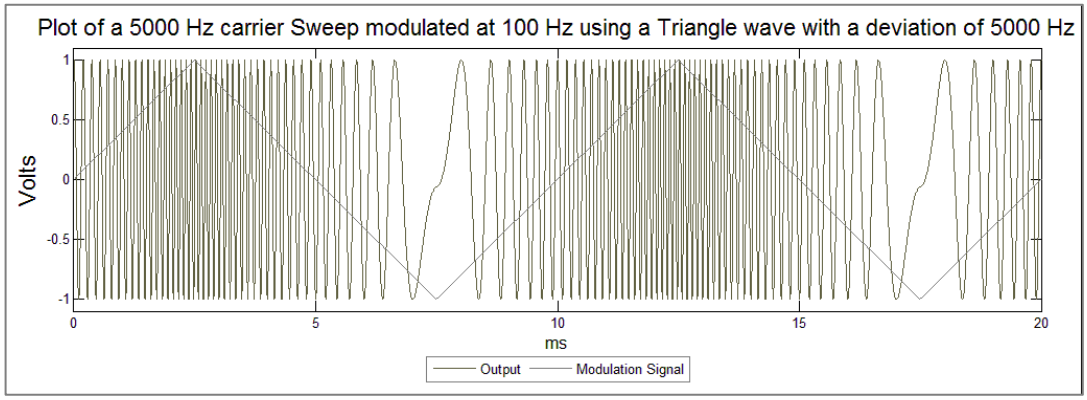


Figure 15: Simulation of Sweep modulation

I/Q Modulation (Optional)

This option extends the SG384's standard modulation suite with In-phase/Quadrature modulation capabilities.

This allows modulation of the front panel N-Type output for frequencies within the range of 400 MHz to 4.05 GHz and supports modulation bandwidths of 100 MHz.

Because of output amplifier limitations, the amplitude setting is limited to +10 dBm during I/Q modulation. This guarantees that the modulator output does exceed the full scale output of the amplifier.

This option provides four BNC connectors on the rear panel. One pair is used for the external inputs, while the second pair provides outputs of the I/Q waveforms. For external operation, the input signals are replicated on the outputs. During times when the internal noise function is selected a facsimile of the noise is present on the I output with the Q output being held at zero.

The inputs are terminated with 50 Ω, and support a signal bandwidth from DC to 100 MHz. A 500 mV level on either input produces full scale output (full scale determined by the present amplitude setting). Any combination of I and Q input levels that when added in quadrature have a level of 500 mV will likewise result in full-scale output.

Figure 16 depicts the relationship between the I and Q levels when added in quadrature and the resulting output magnitude

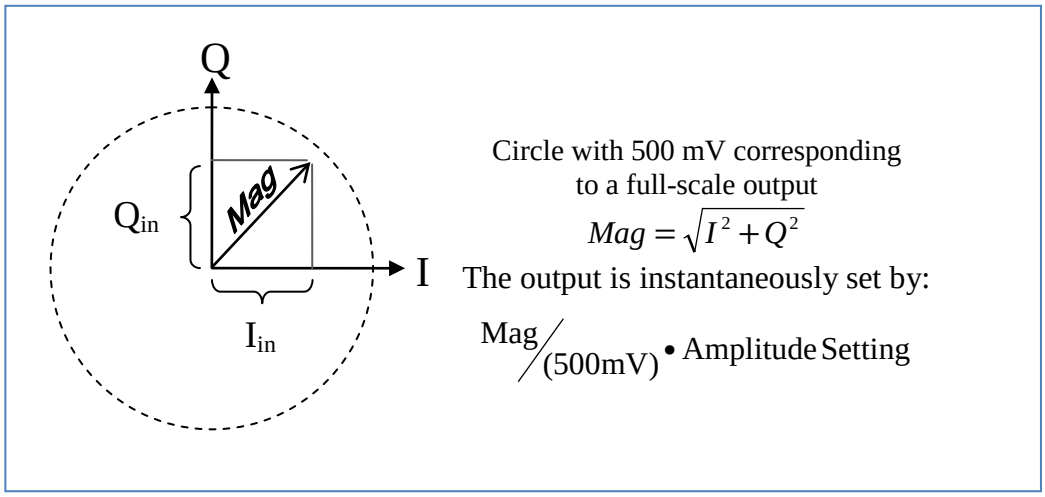


Figure 16: IQ Relationship

The inputs are designed to allow full-scale modulation. Each input is monitored and if either exceeds 525 mV (105 %) the front panel EXT overload LED is turned on and remains on until the condition is removed.

When the inputs are not driven the output theoretically should have no signal present. However carrier feed through and finite input offsets degrade this. These result in a residual carrier error of not more than −40 dBc. For example, if the amplitude is set to −10 dBm the residual carrier will be less than −50 dBm.

When the noise function is selected the SG384 produces a spectral output with a rectangular profile. The width is of the profile is determined by the ENBW setting and may range from 1 µHz to 50 kHz.

To select I/Q modulation, set the modulation type to I/Q and turn on the modulation.

I/Q modulation is not applied to the 8 GHz doubler or BNC outputs.

The two functions available are external and internal noise source.

Modulation Effective Noise Bandwidth (ENBW)

Pressing [MOD RATE] displays the SG384's modulation ENBW and turns on MOD RATE LED.

When the external modulation function is selected there is no rate parameter and the SG384 displays the message “rate etrn”.

When the noise modulation function is selected, the rate determines the bandwidth of the noise. The value may be set using the SELECT/ADJUST arrow keys or via a numeric entry completed with one of the [Hz] unit keys.

Fixed Modulation Deviation

Pressing [MOD DEV] displays the deviation parameter, and turns on the DEVIATION LED.

When the external modulation function is selected, there is no corresponding deviation parameter. The SG384 displays the message “dev predefined”. (The scale is fixed at ±0.5V providing full scale on the I or Q outputs).

With the noise modulation function selected, the output has a fixed crest factor (ratio of peak to RMS) of 14 dB and the SG384 displays a message of “crest fact. 14 dB”.

The following shows two examples using IQ modulation.

Figure 17 shows a 1500 MHz carrier being modulated by 50 and 100MHz I and Q signals, with both set at 0.35V.

(Freq = 1500 MHz, Type = I/Q, Fnc = Ext, External I/Q of 50/100 MHz at 0.35/0.35 V)

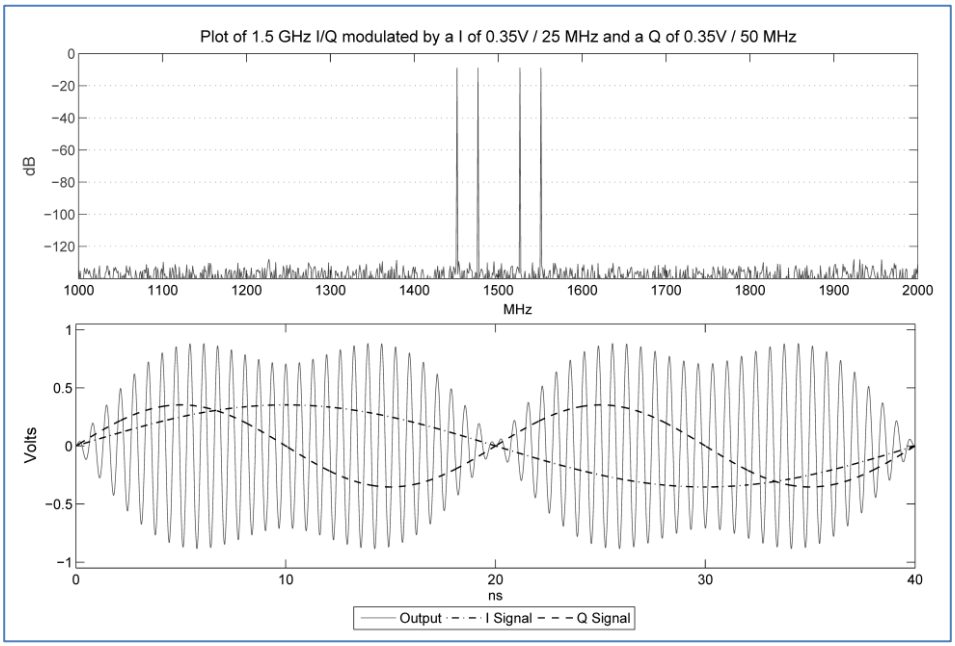


Figure 17: Simulation of I/Q modulation

Figure 18 is a 1500 MHz carrier being modulated by 25 MHz and 100 MHz I and Q signals, with amplitudes of 0.35 and 0.175 volts, respectively.

(Freq = 1500 MHz, Type = I/Q, Fnc = Ext, External I/Q of 25/100 MHz at 0.35/0.175 V)

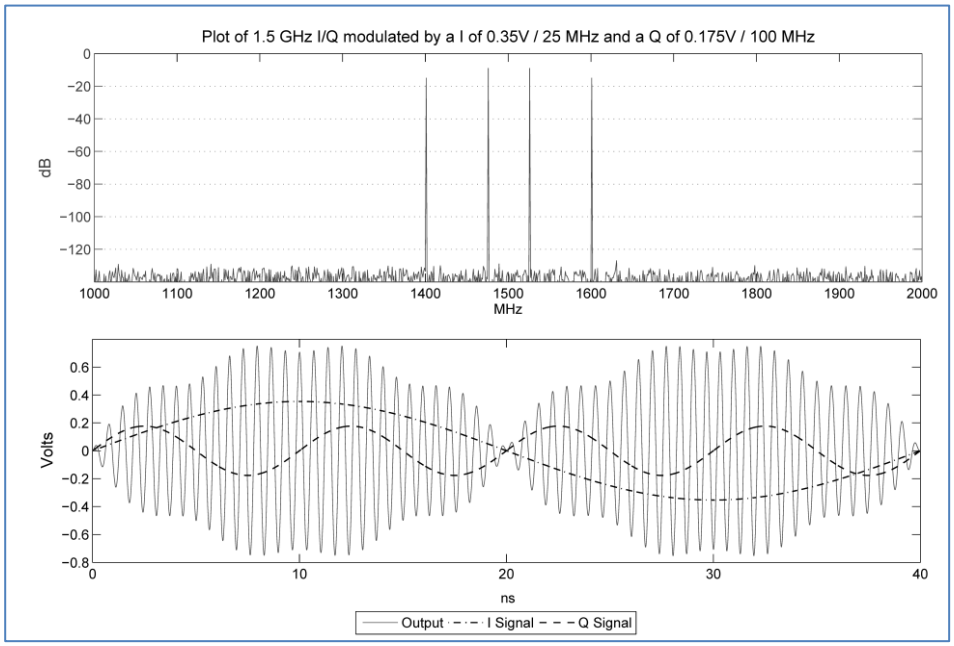


Figure 18: Simulation of I/Q modulation

Secondary (Shift) Parameters

The shifted keys are used to access parameters or functions that are less frequently required. Table 10 gives a summary of the keys.

Table 10: Shifted Key Functions

Label	Primary Key	Function Description
NET	•	Configure Ethernet interface
CAL	+/-	Adjust the timebase, and selects the PLL filter mode
INIT	0	Load default instrument settings
TIMEBASE	1	Displays the timebase configuration
STATUS	2	View TCP/IP (Ethernet), error, or instrument status, as well as running Self-Test
LOCAL	3	Go to local. Enables front panel keys if the unit is in remote mode.
GPIB	4	Configure GPIB interface
RS-232	5	Configure RS-232 interface
DATA	6	Display the most recent data received over any remote interface
REL Φ =0	7	Defines the current phase to be 0 degrees and displays phase parameter (of 0)
PRBS	8	Allows access to the parameters associated with the Pseudo-Random Binary Sequence generator
STEP SIZE	9	Set the incremental value used by the ADJUST keys

Some of the keys in the Numeric Entry section of the front panel have secondary functions associated with them. The names of these functions are printed above the key. For example, the [4] key has the label “RS-232” in light blue text above it.

REL Φ=0

Normalizes the present phase setting to zero and sets the display to the phase parameter. See Phase setting on page 21. The phase of the output is not changed.

PRBS

Sets the PRBS bit length (from 5 to 19). Please see Pulse Modulation section on PRBS Noise Modulation on page 37.

STEP SIZE

Sets and views increment value (used by the ADJUST keys) to an arbitrary value. Please see section Step Size on page 11 for more details.

Timebase

Shows the SG384's installed timebase. This can be the standard ovenized crystal oscillator (OCXO) or an optional rubidium oscillator.

Table 11: Timebase Status Menu

Parameter	Example Display	Description
Oscillator	'Osc. standard'	Indicates which type of timebase is installed.
Rb lock	'Rb stable'	If a rubidium timebase is installed, this item indicates if the rubidium has stabilized.

NET

The NET menu enables the user to configure the TCP/IP based remote interfaces (the IP address, subnet mask, and default router). To see the current TCP/IP parameters use the STATUS menu. Before connecting the SG384 to your LAN, check with your network administrator for the proper configuration of instruments on your network.

The NET menu (summarized in Table 12) has several options. Press the SELECT ◁ and ▷ keys to cycle through the options. Use the MODIFY △ and ▽ keys to change an option. Use the numeric keypad to enter an IP address when appropriate. Note that changes to the TCP/IP configuration do not take effect until the interface is reset or power is cycled.

Table 12: NET Menu Options for TCP/IP Configuration

Parameter	Example Display	Description
TCP/IP	'TCPIP enabled'	Enable or disable all TCP/IP access
DHCP	'DHCP enabled'	Enable or disable the DHCP client to automatically obtain an appropriate TCP/IP configuration from a DHCP server
Static IP	'Static IP enabled'	Enable or disable a static IP configuration.
IP	'IP 192.168.0.5'	IP address to use if static IP is enabled.
Subnet	'Subnet 255.255.0.0'	Subnet mask to use if static IP is enabled.
Default gateway	'Def Gty 192.168.0.1'	Default gateway or router to use for routing packets not on the local network if static IP is enabled
Bare socket interface	'Bare enabled'	Enable or disable raw socket access on TCP/IP port 5025.
Telnet interface	'Telnet enabled'	Enable or disable telnet access on TCP/IP port 5024.
VXI-11 Interface	'Net instr enabled'	Enable or disable the VXI-11 net instrument remote interface.
Link speed	'Speed 100 Base-T'	Set the Ethernet link speed.
Reset	'Reset no'	Select 'Reset yes' and press 'ENTER' to reset the TCP/IP interface to use the latest TCP/IP configuration settings.

TCP/IP Configuration Methods

In order to function properly on an Ethernet based local area network (LAN), the SG384 needs to obtain a valid IP address, a subnet mask, and a default gateway or router address. The SG384 supports three methods for obtaining these parameters: DHCP, Auto-IP, and Static IP. Check with your network administrator for the proper method of configuration of instruments on your network.

If the DHCP client is enabled, the SG384 will try to obtain its TCP/IP configuration from a DHCP server located somewhere on the local network. If the Auto-IP protocol is enabled, the SG384 will try to obtain a valid link-local IP configuration in the 169.254.x.x address space. If the static IP configuration is enabled, the SG384 will use the given TCP/IP configuration. When all three methods are enabled, the TCP/IP configuration will be determined in the following order of preference: DHCP, Auto-IP, and static IP. Given that Auto-IP is virtually guaranteed to succeed, it should be disabled if a static IP configuration is desired.

Please see the Status details on page 50 for details on viewing the TCP/IP address obtained via DHCP or Auto-IP methods.

TCP/IP Based Remote Interfaces

The SG384 supports three TCP/IP based remote interfaces: raw socket, telnet, and VXI-11 net instrument. Raw socket access is available on port 5025. Telnet access is available on port 5024. The VXI-11 interface enables IEEE 488.2 GPIB-like access to the SG384 over TCP/IP. It enables controlled reads and writes and the ability to generate service requests. Most recent VISA instrument software libraries support this protocol.

Link Speed

The SG384's physical Ethernet layer supports 10 Base-T and 100 Base-T link speeds. The default link speed is set to 100 Base-T, but it can be set to 10 Base-T.

Reset the TCP/IP Interface

Note that changes to the TCP/IP configuration do not take effect until the TCP/IP interface is either reset or the instrument is power cycled. To reset the TCP/IP interface, navigate through the NET menu options until "reset no" is displayed. Press the MODIFY △ key to display "reset yes" and then press ENTER. Any active connections will be aborted. The TCP/IP stack will be re-initialized and configured using the latest configuration options.

GPIB

The GPIB menu enables the user to configure the GPIB remote interface. The GPIB menu has several options. Press the SELECT ◁ and ▷ keys to cycle through the options. Use the MODIFY △ and ▽ keys to change an option. Note that changes to the GPIB configuration do not take effect until the interface is reset or the instrument is power cycled. The GPIB menu parameters are summarized in Table 13:

Table 13: GPIB Menu Options

Parameter	Example Display	Description
GPIB	'GPIB enabled'	Enable or disable all GPIB access
Address	'Address 15'	GPIB address
Reset	'Reset no'	Select 'reset yes' and press 'ENTER' to reset the GPIB interface.

GPIB Address

In order to communicate properly on the GPIB bus, the SG384 must be configured with a unique address. Use the Address menu option to set the SG384's GPIB address. Then reset the interface to make sure the new address is active.

Reset the GPIB Interface

Note that changes to the GPIB configuration do not take effect until the GPIB interface is either reset or the instrument is power cycled. To reset the GPIB interface, navigate through the GPIB menu options until "reset no" is displayed. Press the MODIFY △ key to display "reset yes" and press ENTER.

RS-232

The RS-232 menu enables the user to configure the RS-232 remote interface. The RS-232 menu has several options. Press the SELECT ◁ and ▷ keys to cycle through the options. Use the MODIFY △ and ▽ keys to change an option. Note that changes to the RS-232 configuration do not take effect until the interface is reset or the instrument is power cycled. The RS-232 menu parameters are summarized in Table 14.

Table 14: RS-232 Menu Options

Parameter	Example Display	Description
RS-232	'RS-232 enabled'	Enable or disable all RS-232 access
Baud rate	'Baud 11500'	The baud rate to use for RS-232 connections
Reset	'Reset no'	Select 'yes' and press 'ENTER' to reset the RS-232 interface.

RS-232 Configuration

In order to communicate properly over RS-232, the SG384 and the host computer both must be configured to use the same configuration. The SG384 supports the following baud rates: 115200 (default), 57600, 38400, 19200, 9600, and 4800. The rest of the communication parameters are fixed at 8 data bits, 1 stop bit, no parity, and RTS/CTS hardware flow control.

Use the baud rate menu option to set the SG384's baud rate. Then reset the interface to make sure the new baud rate is active.

Reset the RS-232 Interface

Note that changes to the RS-232 configuration do not take effect until the RS-232 interface is either reset or the instrument is power cycled. To reset the RS-232 interface, navigate through the RS-232 menu options until "reset no" is displayed. Press the MODIFY △ key display "reset yes" and press ENTER.

DATA

The DATA function enables the user to see the hexadecimal ASCII characters received by the SG384 from the most recently used remote interface. This functionality is useful when trying to debug problems in communicating with the SG384. Use the MODIFY △ and ▽ keys to scroll through the data. The decimal point indicates the last character received.

STATUS

The STATUS function enables the user to view status information about the SG384. The SG384 has four status menus: TCP/IP status, error status, instrument status, and self test. Use the MODIFY △ and ▽ keys to select the desired status. Then press the SELECT ◁ and ▷ keys to view each item of status.

TCP/IP Status

TCP/IP status contains status information on the current IP configuration of the SG384. Table 15 summarizes the TCP/IP status information reported by the SG384.

Table 15: TCP/IP Status Menu

Parameter	Example Display	Description
Ethernet mac address	'Phy Adr 00.19.b3.02.00.01'	This is the Ethernet mac address assigned to this SG384 at the factory.
Link status	'Connected'	Indicates if the Ethernet hardware has established a link to the network.
IP address	'IP 192.168.0.5'	The current IP address.
Subnet mask	'Subnet 255.255.0.0'	The current subnet mask.
Default gateway	'Def Gty 192.168.0.1'	The current default gateway or router.

Error Status

The error status menu enables the user to view the number and cause of execution and parsing errors. Table 16 summarizes the error status items reported by the SG384. See section Error Codes on page 87 for a complete list of error codes.

Table 16: Error Status Menu

Parameter	Example Display	Description
Error count	'Error cnt 1'	Indicates the number of errors detected.
Error code	'111 Parse Error'	Provides the error number and description of the error.

When an error is generated the front panel error LED is turned on. The ERR LED remains on until the status is interrogated, the unit is re-initialized using INIT, or the SG384 receives the remote command *CLS.

Instrument Status

The instrument status menu enables the user to view the instrument configuration including reports rear panel options.

Table 17: Instrument Status Menu

Parameter	Example Display	Description
Serial Number	'Serial 001013'	Unit serial number
Version	'Version 1.00.10A'	Firmware version
Rear option	'Rear opt. 3'	Indicates which rear option, if any, is installed.

Self Test

The instrument self test runs a series of tests to check the operation of the unit. Three sets of tests are run. They are summarized in Table 18.

Table 18: Instrument Self Test

Self Test Description
Tests communication to various peripherals on the motherboard including GPIB chip, the PLL chips, the DDS chips, the octal DACs, the FPGA, and the serial EEPROM.

After the self test completes, the unit is set to default instrument settings. If errors are encountered, they will be reported on the front-panel display when detected. The errors detected are stored in the instrument error buffer and may be accessed via the error status menu after the self test completes. See section Error Codes on page 87 for a complete list of error codes.

LOCAL

When the SG384 is in remote mode, the REM LED is highlighted and front-panel instrument control is disabled. Pressing the [3] (LOCAL) key re-enables local front-panel control.

INIT

Executing the INIT function forces the SG384 to default settings. This is equivalent to a Recall 0 or executing the *RST remote command. See Factory Default Settings on page 52 for a list of the SG384's default settings.

CAL

This accesses the internal timebase user calibration parameter or the RF PLL Noise Mode setting. The user calibration parameter allows adjustment of the timebase over a range of ± 2 ppm (10 MHz ± 20 Hz).

The RF PLL Mode has two settings RF PLL 1 and 2. RF PLL1 optimizes the noise floor of the output within 100 kHz of the carrier. This is the default setting.

RF PLL 2 optimizes the noise floor of the output for offset greater than 100 kHz from carrier. (Please see the Graph 3: Single Sideband Phase Noise for RF PLL Modes on page xvi).

Factory Default Settings

The factory default settings are listed in Table 19. The SG384 may be forced to assume its factory default settings by power cycling the unit with the [BACK SPACE] key depressed. This forces all instrument settings except for communication parameters to the factory defaults. It is similar to the INIT secondary function and the *RST remote command, which also reset the unit to factory default settings. However the Factory Reset also performs these additional actions:

1. Resets *PSC to 1
2. Forces nonvolatile copies of *SRE and *ESE to 0.
3. Resets all stored settings from 1 to 9 back to default settings

Table 19: SG384 Factory Default Settings

Parameter	Value	Step Size
Display	Frequency	
Frequency	10 MHz	1 Hz
Phase	0 Degrees	1 Degree
Amplitude (BNC, NTYPE, Doubler)	0 dBm 0.224 V_{RMS} 0.632 V_{PP}	1 dBm 0.1 V_{RMS} 0.1 V_{PP}
Amplitude (Clock Option)	0.4 V_{PP}	0.1 V_{PP}
Offset (BNC, Clock, Rear DAC)	0 V	0.1 V
RF PLL Filter Mode	1	
Modulation On/Off	Off	
Modulation Type	FM	
Modulation Function (AM/FM/PM)	Sine	
Modulation Function (Sweep)	Triangle	
Modulation Function (Pulse/Blank)	Square	
Modulation Function (I/Q)	External	
Modulation Rate (AM/FM/PM)	1 kHz	1 kHz
Modulation Rate (Sweep)	100 Hz	10 Hz
Modulation Input Coupling	DC	
AM Depth	50 %	10 %
FM Deviation	1 kHz	1 kHz
PM Deviation	10 Degrees	10 Degrees
Sweep Deviation	1 MHz	1 MHz
AM RMS Noise Depth	10 %	10 %
FM RMS Noise Deviation	1 kHz	1 kHz
PM RMS Noise Deviation	10 Degrees	10 Degrees
Pulse/Blank Period	1000 µs	100 µs
Pulse/Blank Width	1 µs	0.1 µs
PRBS Length	9	
PRBS Period	1 µs	0.1 µs

The factory default settings of the various communications interfaces for the SG384 are listed in Table 20. The SG384 may be forced to assume its factory default communication settings by power cycling the unit with the [NET] key depressed.

Table 20: SG384 Factory Default Settings for Communications Parameters

Parameter	Setting
RS-232	Enabled
RS-232 Baud Rate	115200
GPIB	Enabled
GPIB Address	27
TCP/IP	Enabled
DHCP	Enabled
Auto-IP	Enabled
Static IP	Enabled
IP	0.0.0.0
Subnet Mask	0.0.0.0
Default Gateway	0.0.0.0
Bare (Raw) Socket Interface at TCP/IP port 5025	Enabled
Telnet Interface at TCP/IP port 5024	Enabled
VXI-11 Net Instrument Interface	Enabled
Ethernet Speed	100 Base-T

Remote Programming

Introduction

The SG384 may be remotely programmed via the GPIB interface, the RS-232 serial interface, or the LAN Ethernet interface. Any host computer interfaced to the SG384 can easily control and monitor the operation of the SG384.

Interface Configuration

All of the SG384 interface configuration parameters can be accessed via the front panel through shifted functions dedicated to the interface. Table 21 identifies the shifted functions that are used to configure each interface.

Table 21: SG384 Interface Configuration

Shifted Function	Interface Configuration
NET [•]	LAN, TCP/IP interface
GPIB [4]	GPIB 488.2 interface
RS-232 [5]	RS-232 serial interface

Each interface's configuration is accessed by pressing [SHIFT] followed by one of the interface keys ([NET], [GPIB], or [RS-232]). Once a given interface configuration is activated, parameters for the interface are selected by successive SELECT ▷ key presses. For example, pressing [SHIFT], [RS-232] activates the RS-232 configuration. The first menu item is RS-232 Enable/Disable. Pressing SELECT ▷ moves the selection to RS-232 baud rate.

Once a parameter is selected, it is modified by pressing the ADJUST △ and ▽ keys. The only exception to this is for selections that require an internet address, such as static IP address, network mask, and default gateway address. In this case the address is modified by entering the new address with the numeric keys and pressing [ENTER].

All interfaces are enabled by default, but each interface may be disabled individually if desired. Any modifications made to an interface do not take effect until the interface is reset or the unit is power cycled.

GPIB

The SG384 comes with an IEEE 488 standard port for communicating over GPIB. The port is located on the rear panel of the SG384. The configuration parameters for the GPIB interface are shown in Table 22.

Table 22: GPIB Configuration

Interface Parameter	Default	Meaning
GPIB Enable/Disable	Enabled	Enable or disable the interface
GPIB Address (0-30)	27	Primary GPIB address.
Reset interface (Yes/No)	No	Force a reset of the interface.

Any changes made will not take effect until the interface is reset or the unit is power cycled.

RS-232

The SG384 comes standard with an RS-232 communications port. The port is located on the rear panel of the SG384. The configuration parameters for the RS-232 interface are shown in Table 23.

Table 23: RS-232 Configuration

Interface Parameter	Default	Meaning
RS-232 enable/disable	Enabled	Enable or disable the interface
Baud rate (4800-115200)	115200	RS-232 baud rate
Reset interface (yes/no)	No	Force a reset of the interface.

The RS-232 interface connector is a standard 9 pin, type D, female connector configured as a DCE (transmit on pin 2, receive on pin 3). The factory default communication parameters are set to: 115200 baud rate, 8 data bits, 1 stop bit, no parity, RTS/CTS hardware flow control. All of these communication parameters are fixed except for the baud rate. Any changes made to the interface configuration will not take effect until the interface is reset or the unit is power cycled.

LAN

The SG384 comes standard with an RJ-45 network communications port located on the rear panel of the SG384. The port may be used to communicate with the SG384 over a 10/100 Base-T Ethernet connected network or LAN. Before connecting the SG384 to your LAN, check with your network administrator for the proper method of configuration of networked instruments on your network. The TCP/IP configuration options for the LAN interface are shown in Table 24.

Table 24: LAN Configuration

Interface Parameter	Default	Meaning
TCP/IP Enable/Disable	Enabled	Enable or disable all TCP/IP based interfaces.
DHCP Enable/Disable	Enabled	Enable or disable automatic network configuration via DHCP.
Auto-IP Enable/Disable	Enabled	Enable or disable automatic network configuration in the 169.254.x.x internet address space if DHCP fails or is disabled.
Static IP Enable/Disable	Enabled	Enable manual configured network configuration in the event that the automatic configuration fails or is disabled.
IP Address	0.0.0.0	Static IP address to use when manual configuration is active.
Subnet Address	0.0.0.0	Network mask to use when manual configuration is active. The network mask is used to determine which IP addresses are on the local network.
Default Gateway	0.0.0.0	Default gateway or router to use when manual configuration is active. The gateway is the IP address that packets are sent to if the destination IP address is not on the local network.
Bare Socket Enable/Disable	Enabled	Enable or disable raw socket access to the SG384 via TCP port 5025.
Telnet Enable/Disable	Enabled	Enable or disable access to the SG384 via telnet at TCP port 5024.
Net Instr. Enable/Disable	Enabled	Enable or disable access to the SG384 via VXI-11 net instrument protocols.
Ethernet Speed 10/100	100 Base-T	Ethernet physical layer link speed.
Reset interface (Yes/No)	No	Force a reset of the interface.

The SG384 supports automatic and static network configuration. When more than one configuration is enabled, the SG384 selects network configuration parameters with the following priority: DHCP, Auto-IP, and finally Manual. Note that since Auto-IP will virtually always succeed, it should be disabled if static configuration is desired. Any changes made to the interface configuration will not take effect until the interface is reset or the unit is power cycled.

Network Security

Network security is an important consideration for all TCP/IP networks. Please bear in mind that the SG384 does NOT provide security controls, such as passwords or encryption, for controlling access to the SG384. If such controls are needed, you must provide it at a higher level on your network. This might be achieved, for example, by setting up a firewall and operating the SG384 behind it.

Front-Panel Indicators

To assist in programming, the SG384 has three front panel indicators located under the INTERFACE section: REM, ACT, and ERR. The REM LED is on when the SG384 is in remote lock out. In this mode, the front panel interface is locked out and the SG384 can only be controlled via the remote interface. To go back to local mode, the user must press the LOCAL key, [3]. The ACT LED serves as an activity indicator that flashes every time a character is received or transmitted over one of the remote interfaces.

The ERR LED will be highlighted when a remote command fails to execute due to illegal syntax or invalid parameters. The user may view the cause of errors from the front panel by pressing the keys [SHIFT], [STATUS], sequentially. Next press ADJUST △ until the display reads “Error Status”. Finally, press SELECT ▷ successively, to view the total error count followed by the individual errors. The error codes are described in section Error Codes on page 87.

Command Syntax

Communications with the SG384 uses ASCII characters. All commands are 4-characters long and are case-insensitive. Standard IEEE-488.2 defined commands begin with the '*' character followed by 3 letters. SG384 specific commands are composed of 4 letters.

The four letter mnemonic (shown in capital letters) in each command sequence specifies the command. The rest of the sequence consists of parameters.

Commands may take either *set* or *query* form, depending on whether the '?' character follows the mnemonic. *Set only* commands are listed without the '?', *query only* commands show the '?' after the mnemonic, and *query optional* commands are marked with a '(?)'.

Parameters shown in { } and [ ] are not always required. Parameters in { } are required to set a value, and are omitted for queries. Parameters in [ ] are optional in both set and query commands. Parameters listed without any surrounding characters are always required.

Do NOT send () or {} or [] or spaces as part of the command.

The command buffer is limited to 768 bytes, with 25 byte buffers allocated to each of up to 3 parameters per command. If the command buffer overflows, both the input and output buffers will be flushed and reset. If a parameter buffer overflows, a command error will be generated and the offending command discarded.

Commands are terminated by a semicolon, a <CR> (ASCII 13), or a <LF> (ASCII 10). If the communications interface is GPIB, then the terminating character may optionally be accompanied by an EOI signal. If the EOI accompanies a character other than a <LF>, a <LF> will be appended to the command to terminate it. Execution of the command does not begin until a command terminator is received.

Aside from communication errors, commands may fail due to either syntax or execution errors. Syntax errors can be detected by looking at bit 5 (CME) of the event status register (*ESR?). Execution errors can be detected by looking at bit 4 (EXE) of the event status register. In both cases, an error code, indicating the specific cause of the error, is appended to the error queue. The error queue may be queried with the LERR? command. Descriptions of all error codes can be found in the section Error Codes, starting on page 87.

Parameter Conventions

The command descriptions use parameters, such as i, f, and v. These parameters represent integers or floating point values expected by the command. The parameters follow the conventions summarized in Table 25.

Table 25: Command Parameter Conventions

Parameter	Meaning
i, j, k	An integer value
f	A floating point value representing a frequency in Hz.
p	A floating point value representing a phase in degrees.
t	A floating point value representing time in seconds.
v	A floating point value representing voltage in volts.
u	An identifier of units. Allowed units depend on the type as identified below:

Type	Allowed Units
Amplitude	‘dBm’, ‘rms’, ‘Vpp’
Frequency	‘GHz’, ‘MHz’, ‘kHz’, or ‘Hz’
Time	‘ns’, ‘us’, ‘ms’, or ‘s’

Numeric Conventions

Floating point values may be decimal (‘123.45’) or scientific (‘1.2345e2’). Integer values may be decimal (‘12345’) or hexadecimal (‘0x3039’).

Abridged Index of Commands

Common IEEE-488.2 Commands

*CAL?	Page 63	Run auto calibration routine
*CLS	Page 63	Clear Status
*ESE(?){i}	Page 63	Standard Event Status Enable
*ESR?	Page 63	Standard Event Status Register
*IDN?	Page 63	Identification String
*OPC(?)	Page 63	Operation Complete
*PSC(?){i}	Page 64	Power-on Status Clear
*RCL i	Page 64	Recall Instrument Settings
*RST	Page 64	Reset the Instrument
*SAV i	Page 64	Save Instrument Settings
*SRE(?){i}	Page 64	Service Request Enable
*STB?	Page 65	Status Byte
*TRG	Page 65	Trigger a delay
*TST?	Page 65	Self Test
*WAI	Page 65	Wait for Command Execution

Status and Display Commands

DISP(?){i}	Page 66	Display
INSE(?){i}	Page 66	Instrument Status Enable
INSR?	Page 66	Instrument Status Register
LERR?	Page 67	Last Error
OPTN? i	Page 67	Installed Options
TEMP?	Page 67	Temperature of the RF block
TIMB?	Page 67	Timebase

Signal Synthesis Commands

AMPC(?){v}	Page 69	Amplitude of Clock
AMPH(?){v}[u]	Page 69	Amplitude of HF (RF Doubler)
AMPL(?){v}[u]	Page 69	Amplitude of LF (BNC Output)
AMPR(?){v}[u]	Page 69	Amplitude of RF (N-Type Output)
ENBC(?){i}	Page 70	Enable Clock
ENBH(?){i}	Page 70	Enable HF (RF Doubler)
ENBL(?){i}	Page 70	Enable LF (BNC Output)
ENBR(?){i}	Page 70	Enable RF (N-Type Output)
FREQ(?){f}[u]	Page 70	Frequency
OFSC(?){v}	Page 70	Offset of Clock
OFSD(?){v}	Page 70	Offset of Rear DC
OFSL(?){v}	Page 70	Offset of LF (BNC Output)
PHAS(?){p}	Page 71	Phase
RPHS	Page 71	Rel Phase

Modulation Commands

ADEP(?){d}	Page 73	AM Modulation Depth
ANDP(?){d}	Page 73	AM Noise Modulation Depth
COUP(?){i}	Page 73	Modulation Coupling
FDEV(?){f}[u]	Page 73	FM Deviation
FNDV(?){f}[u]	Page 73	FM Noise Deviation
MFNC(?){i}	Page 74	Modulation Function for AM/FM/ΦM
MODL(?){i}	Page 74	Modulation Enable
PDEV(?){p}	Page 74	ΦM Deviation
PDTY(?){d}	Page 74	Pulse/Blank Duty Factor
PFNC(?){i}	Page 74	Pulse Modulation Function
PNDV(?){p}	Page 75	ΦM Noise Deviation
PPER(?){t}[u]	Page 75	Pulse/Blank Period
PRBS(?){i}	Page 75	PRBS Length for Pulse/Blank Modulation
PWID(?){t}[u]	Page 75	Pulse/Blank Width
QFNC(?){i}	Page 75	IQ Modulation Function
RATE(?){f}[u]	Page 76	Modulation Rage for AM/FM/ΦM
RPER(?){t}[u]	Page 76	PRBS Period for Pulse/Blank Modulation
SDEV(?){f}[u]	Page 76	Sweep Deviation
SFNC(?){i}	Page 76	Sweep Modulation Function
SRAT(?){f}[u]	Page 76	Modulation Sweep Rate
TYPE(?){i}	Page 77	Modulation Type

List Commands

LSTC? i	Page 78	List Create
LSTD	Page 78	List Delete
LSTE(?){i}	Page 78	List Enable
LSTI(?){i}	Page 78	List Index
LSTP(?) i {,<st>}	Page 78	List Point
LSTS?	Page 79	List Size

Interface Commands

EMAC?	Page 79	Ethernet MAC Address
EPHY(?){i}	Page 79	Ethernet Physical Layer Configuration
IFCF(?)i{,j}	Page 79	Interface Configuration
IFRS i	Page 80	Interface Reset
IPCF? i	Page 80	Active TCP/IP Configuration
LCAL	Page 80	Go to Local
LOCK?	Page 80	Request Lock
REMT	Page 80	Go to Remote
UNLK?	Page 80	Release Lock
XTRM i{,j,k}	Page 80	Interface Terminator

Detailed Command List

Common IEEE-488.2 Commands

*CAL? Auto calibration

This command currently does nothing and returns 0.

*CLS Clear Status

Clear Status immediately clears the ESR and INSR registers as well as the LERR error buffer.

*ESE(?){i} Standard Event Status Enable

Set (query) the Standard Event Status Enable register {to i}. Bits set in this register cause ESB (in STB) to be set when the corresponding bit is set in the ESR register.

*ESR? Standard Event Status Register

Query the Standard Event Status Register. Upon executing a *ESR? query, the returned bits of the *ESR register are cleared. The bits in the ESR register have the following meaning:

Bit	Meaning
0	OPC – operation complete
1	Reserved
2	QYE – query error
3	DDE – device dependent error
4	EXE – execution error
5	CME – command error
6	Reserved
7	PON – power-on

Example

*ESR? A return of ‘176’ would indicate that PON, CME, and EXE are set.

*IDN? Identification String

Query the instrument identification string.

Example

*IDN? Returns a string similar to ‘Stanford Research Systems,SG384,s/n004025,ver1.00.0B’

*OPC(?) Operation Complete

The set form sets the OPC flag in the ESR register when all prior commands have completed. The query form returns ‘1’ when all prior commands have completed, but does not affect the ESR register.

*PSC(?){i} Power-on Status Clear

Set (query) the Power-on Status Clear flag {to i}. The Power-on Status Clear flag is stored in nonvolatile memory in the SG384, and thus, maintains its value through power-cycle events.

If the value of the flag is 0, then the Service Request Enable and Standard Event Status Enable Registers (*SRE, *ESE) are stored in non-volatile memory, and retain their values through power-cycle events. If the value of the flag is 1, then these two registers are cleared upon power-cycle.

Example

*PSC 1	Set the Power-on Status Clear to 1.
*PSC?	Returns the current value of Power-on Status Clear.

*RCL i Recall Instrument Settings

Recall instrument settings from location i. The parameter i may range from 0 to 9. Locations 1 to 9 are for arbitrary use. Location 0 is reserved for the recall of default instrument settings.

Example

*RCL 3	Recall instruments settings from location 3.

*RST Reset the Instrument

Reset the instrument to default settings. This is equivalent to *RCL 0. It is also equivalent to pressing the keys [SHIFT], [INIT], [ENTER on the front panel. See Factory Default Settings on page 52 for a list of default settings.

Example

*RST	Resets the instrument to default settings

*SAV i Save Instrument Settings

Save instrument settings to location i. The parameter i may range from 0 to 9. However, location 0 is reserved for current instrument settings. It will be overwritten after each front panel key press.

Example

*SAV 3	Save current settings to location 3.

*SRE(?){i} Service Request Enable

Set (query) the Service Request Enable register {to i}. Bits set in this register cause the SG384 to generate a service request when the corresponding bit is set in the STB register.

*STB? Status Byte

Query the standard IEEE 488.2 serial poll status byte. The bits in the STB register have the following meaning:

Bit	Meaning
0	INSB – INSR summary bit
1	Reserved
2	Reserved
3	Reserved
4	MAV – message available
5	ESB – ESR summary bit
6	MSS – master summary bit
7	Reserved

Example

*STB? A return of '113' would indicate that INSB, MAV, ESB, and MSS are set. INSB indicates that an enabled bit in INSR is set. MAV indicates that a message is available in the output queue. ESB indicates that an enabled bit in ESR is set. MSS reflects the fact that at least one of the summary enable bits is set and the instrument is requesting service.

*TRG Trigger

When the SG384 is configured for list operation, this command initiates a trigger. Instrument settings at the current list index are written to the instrument and the index is incremented to the next list entry.

*TST? Self Test

Runs the instrument self test and returns 0 if successful. Otherwise it returns error code 17 to indicate that the self test failed. Use the LERR? command to determine the cause of the failure.

*WAI Wait for Command Execution

The instrument will not process further commands until all prior commands including this one have completed.

Example

*WAI Wait for all prior commands to execute before continuing.

Status and Display Commands

DISP(?){i} Display

Set (query) the current display value {to i}. The parameter i selects the display type.

i	Display
0	Modulation Type
1	Modulation Function
2	Frequency
3	Phase
4	Modulation Rate or Period
5	Modulation Deviation or Duty Cycle
6	RF N-type Amplitude
7	BNC Amplitude
8	RF Doubler Amplitude
9	Clock Amplitude
10	BNC Offset
11	Rear DC Offset
12	Clock Offset

Example

DISP 2 Show carrier frequency

INSE(?){i} Instrument Status Enable

Set (query) the Instrument Status Enable register {to i}. }. Bits set in this register cause INSB (in STB) to be set when the corresponding bit is set in the INSR register.

INSR? Instrument Status Register

Query the Instrument Status Register. Upon executing a INSR? query, the returned bits of the INSR register are cleared. The bits in the INSR register have the following meaning:

Bit	Meaning
0	20MHZ_UNLK – 20 MHz PLL unlocked.
1	100MHZ_UNLK – 100 MHz PLL unlocked.
2	19MHZ_UNLK – 19 MHz PLL unlocked.
3	1GHZ_UNLK – 1 GHz PLL unlocked.
4	4GHZ_UNLK – 4 GHz PLL unlocked.
5	NO_TIMEBASE – installed timebase is not oscillating.
6	RB_UNLOCK – the installed Rubidium oscillator is unlocked.
7	Reserved
8	MOD_OVLD – external modulation overloaded.
9	IQ_OVLD – external IQ modulation overloaded.
10-15	Reserved

Example

INSR? A return of ‘257’ would indicate that an external modulation overload was detected and the 20 MHz PLL came unlocked.

LERR? Last Error

Query the last error in the error buffer. Upon executing a LERR? query, the returned error is removed from the error buffer. See the section Error Codes later in this chapter for a description of the possible error codes returned by LERR?. The error buffer has space to store up to 20 errors. If more than 19 errors occur without being queried, the 20th error will be 254 (Too Many Errors), indicating that errors were dropped.

OPTN? i Installed Options

Query whether option i is installed. Returns 1 if it is installed, otherwise 0. The parameter i identifies the option.

i	Option
1	Rear clock outputs
2	RF doubler and DC outputs
3	IQ modulation inputs and outputs
4	OCXO timebase
5	Rubidium timebase

TEMP? Temperature

Query the current temperature of the RF output block in degrees C.

TIMB? Timebase

Query the current timebase for the SG384. The returned value identifies the timebase.

Value	Meaning
0	Internal timebase
1	OCXO timebase
2	Rubidium timebase
3	External timebase

Signal Synthesis Commands

Signal synthesis commands enable the user to set the frequency, amplitude, and phase of the outputs. Basic configuration can be achieved by following the steps as outlined in Table 26.

Table 26: SG384 Basic Signal Configuration

Action	Relevant Commands
Set frequency	FREQ
Set amplitude	AMPL, AMPR, AMPC, AMPH
Set offset	OFSL, OFSC, OFSD
Adjust phase	PHAS, RPHS

All of these commands are described in detail below.

AMPC(?){v} Amplitude of Clock

Set (query) the amplitude of the rear clock output {to v} in V_{pp}. Unlike the other amplitude commands, units are always V_{pp}.

AMPH(?){v}[u] Amplitude of HF (RF Doubler)

Set (query) the amplitude of the rear RF doubler {to v}. If omitted, units default to dBm.

Example

AMPH -5.0	Set the rear RF doubler amplitude to –5.0 dBm.
AMPH 0.1 RMS	Set the rear RF doubler amplitude to 0.1 V_{rms}.
AMPH?	Query the rear RF doubler amplitude in dBm.
AMPH? VPP	Query the rear RF doubler amplitude in V_{pp}.

AMPL(?){v}[u] Amplitude of LF (BNC Output)

Set (query) the amplitude of the low frequency BNC output {to v}. If omitted, units default to dBm.

Example

AMPL -1.0	Set the BNC output amplitude to –1.0 dBm.
AMPL 0.1 RMS	Set the BNC output amplitude to 0.1 V_{rms}.
AMPL?	Query the BNC output amplitude in dBm.

AMPR(?){v}[u] Amplitude of RF (N-Type Output)

Set (query) the amplitude of the N-type RF output {to v}. If omitted, units default to dBm.

Example

AMPR -3.0	Set the N-type RF output amplitude to –3.0 dBm.
AMPR 0.1 RMS	Set the N-type RF output amplitude to 0.1 V_{rms}.
AMPR?	Query the N-type RF output amplitude in dBm.

ENBC(?){i} Enable Clock

Set (query) the enable state of the rear clock output {to i}. If i is 0, the clock output is stopped in a low state. If i is 1, the clock is enabled and oscillating at the carrier frequency. Note that the query returns the current state of the output. It may return 0 even if a 1 was sent if the output is not active at the current frequency (i.e. $F_{carrier} > 4.05$ GHz).

ENBH(?){i} Enable HF (RF Doubler)

Set (query) the enable state of the rear RF doubler output {to i}. If i is 0, the RF doubler is disabled and turned off. If i is 1, the rear RF doubler is enabled and operating at the programmed amplitude for the output. Note that the query returns the current state of the output. It may return 0 even if a 1 was sent if the output is not active at the current frequency (i.e. $F_{carrier} < 4.05$ GHz).

ENBL(?){i} Enable LF (BNC Output)

Set (query) the enable state of the low frequency BNC output {to i}. If i is 0, the BNC output is disabled and turned off. If i is 1, the rear RF doubler is enabled and operating at the programmed amplitude for the output. Note that the query returns the current state of the output. It may return 0 even if a 1 was sent if the output is not active at the current frequency (i.e. $F_{carrier} > 62.5$ MHz).

ENBR(?){i} Enable RF (N-Type Output)

Set (query) the enable state of the N-type RF output {to i}. If i is 0, the N-type RF output is disabled and turned off. If i is 1, the N-type RF output is enabled and operating at the programmed amplitude for the output. Note that the query returns the current state of the output. It may return 0 even if a 1 was sent if the output is not active at the current frequency (i.e. $F_{carrier} < 950$ kHz).

FREQ(?){f}[u]Frequency

Set (query) the carrier frequency {to f}. If omitted, units default to Hz.

Example

FREQ 100e6	Set the frequency to 100 MHz.
FREQ 100 MHz	Also sets the frequency to 100 MHz.
FREQ ?	Returns the current frequency in Hz.
FREQ? MHz	Returns the current frequency in MHz

OFSC(?){v} Offset of Clock

Set (query) the offset voltage of the rear clock output {to v} in volts.

OFSD(?){v} Offset of Rear DC

Set (query) the offset voltage of the rear DC output {to v} in volts.

OFSL(?){v} Offset of LF (BNC Output)

Set (query) the offset voltage of the low frequency BNC output {to v} in volts.

PHAS(?){p} Phase

Set (query) the phase of the carrier{to p}. The phase will track to ±360°, but it may only be stepped by 360° in one step. Thus, if the phase is currently 360°, setting the phase to –90° will fail because the phase step is larger than 360°. On the other hand, setting the phase to 370° will succeed but the reported phase will then be 10°.

Example

PHAS 90.0	Set the phase to 90 degrees.
PHAS -10.0	Set the phase to –10 degrees.

RPHS Rel Phase

Make the current phase of the carrier 0°.

Modulation Commands

Modulation commands enable the user to configure different type of modulations of the carrier. Basic configuration can be achieved by following the steps outlined in Table 27.

Table 27: SG384 Basic Modulation Configuration

Modulation	Configuration	Relevant Commands
On/Off	Enable modulation	MODL
External	AC/DC input coupling	COUP
AM	Select AM modulation	TYPE 0
	Modulation function	MFNC
	Mod. rate / Noise bandwidth	RATE
	Deviation	ADEP, ANDP
FM	Select FM modulation	TYPE 1
	Modulation function	MFNC
	Mod. rate / Noise bandwidth	RATE
	Deviation	FDEV, FNDV
ΦM	Select ΦM modulation	TYPE 2
	Modulation function	MFNC
	Mod. rate / Noise bandwidth	RATE
	Deviation	PDEV, PNDV
Sweep	Select frequency sweep	TYPE 3
	Modulation function	SFNC
	Modulation rate	SRAT
	Deviation	SDEV
Pulse/Blank	Select pulse/blank mod.	TYPE 4 or TYPE 5
	Modulation function	PFNC
	Pulse period	PPER
	Pulse width	PWID or PDTY
	PRBS period	RPER
	PRBS length	PRBS
IQ	Select IQ modulation	TYPE 6
	Modulation function	QFNC
	Noise bandwidth	RATE

All of these commands are described in detail below.

ADEP(?){d} AM Modulation Depth

Set (query) the AM modulation depth {to d} in percent.

Note: see ANDP command if noise is the selected modulation function.

Example

ADEP 90.0	Set the depth to 90 %.
ADEP?	Query the current depth in percent.

ANDP(?){d} AM Noise Modulation Depth

Set (query) the AM noise modulation depth {to d} in percent. The value controls the rms depth of the modulation, not the peak deviation as the ADEP command does.

Note: see ADEP command for all modulation functions other than noise.

Example

ANDP 10.0	Set the rms noise depth to 10 %.
ANDP?	Query the current rms noise depth in percent.

COUP(?){i} Modulation Coupling

Set (query) the coupling of the external modulation input {to i}. If i is 0, the input is AC coupled. If i is 1, the input is DC coupled. This setting has no affect on the input if pulse modulation is active. In that case the coupling is always DC.

FDEV(?){f}[u] FM Deviation

Set (query) the FM deviation {to f}. If omitted, units default to Hz.

Note: see FNDV command if noise is the selected modulation function.

Example

FDEV 10e3	Set the FM deviation to 10 kHz.
FDEV?	Query the current FM deviation in Hz.
FDEV 1 kHz	Set the FM deviation to 1 kHz.

FNDV(?){f}[u] FM Noise Deviation

Set (query) the FM noise deviation {to f}. If omitted, units default to Hz. The value controls the rms deviation of the modulation, not the peak deviation as the FDEV command does.

Note: see FDEV command for all modulation functions other then noise.

Example

FNDV 10e3	Set the rms FM noise deviation to 10 kHz.
FNDV?	Query the current rms FM noise deviation in Hz.
FNDV 1 kHz	Set the rms FM noise deviation to 1 kHz.

MFNC(?){i} Modulation Function for AM/FM/ΦM

Set (query) the modulation function or AM/FM/ΦM {to i}. The parameter i may be set to one of the following values:

i	Modulation Function
0	Sine wave
1	Ramp
2	Triangle
3	Square
4	Noise
5	External

Note: see SFNC, PFNC, and QFNC commands for sweeps, pulse/blank, and IQ modulations respectively.

MODL(?){i} Modulation Enable

Set (query) the enable state of modulation {to i}. If i is 0, modulation is disabled. If i is 1, modulation is enabled. This command may fail if the current modulation type is not allowed at current settings. For example, pulse modulation is not allowed at frequencies where the RF doubler is active.

PDEV(?){p} ΦM Deviation

Set (query) the ΦM deviation {to p} in degrees.

Note: see PNDV command if noise is the selected modulation function.

Example

PDEV 45.0	Set the ΦM deviation to 45.0 degrees.
PDEV?	Query the current ΦM deviation.

PDTY(?){d} Pulse/Blank Duty Factor

Set (query) the duty factor for pulse/blank modulation {to d} in percent. This value controls pulse modulation when the selected waveform is square (see PFNC). Use PWID? to determine the actual pulse width in time.

Example

PDTY 10	Set the duty factor to 10 %.
PDTY?	Query the current duty factor.

PFNC(?){i} Pulse Modulation Function

Set (query) the modulation function for pulse/blank modulation {to i}. The parameter i may be set to one of the following values:

i	Modulation Function
3	Square
4	Noise (PRBS)
5	External

Note: see MFNC, SFNC, and QFNC commands for AM/FM/ΦM, sweeps, and IQ modulations respectively.

PNDV(?){p} ΦM Noise Deviation

Set (query) the ΦM noise deviation {to p} in degrees. The value controls the rms deviation of the modulation, not the peak deviation as the PDEV command does.

Note: see PDEV command for all modulation functions other than noise.

Example

PNDV 10.0	Set the rms ΦM noise deviation to 10.0 degrees.
PNDV?	Query the current rms ΦM noise deviation.

PPER(?){t}[u] Pulse/Blank Period

Set (query) the pulse/blank modulation period {to t}. If omitted, units default to seconds. This value controls pulse modulation when the selected waveform is square (see PFNC).

Example

PPER 1e-3	Set the pulse period to 1 ms.
PPER?	Query the current pulse period in seconds.

PRBS(?){i} PRBS Length for Pulse/Blank Modulation

Set (query) the PRBS length for pulse/blank modulation {to i}. The parameter i may range from 8 to 19. It defines the number of bits in the PRBS generator. A value of 8, for example, means the generator is 8 bits wide. It will generate a sequence of pseudo random bits which repeats every $2^8 - 1$ bits. This value controls pulse modulation when the selected waveform is noise (see PFNC).

Example

PRBS 10	Set the PRBS length to 10.
PRBS?	Query the current PRBS length.

PWID(?){t}[u] Pulse/Blank Width

Set (query) the pulse/blank modulation width (duty cycle) {to t}. If omitted, units default to seconds. This value controls pulse modulation when the selected waveform is square (see PFNC).

Example

PWID 1e-6	Set the pulse width to 1 μs.
PWID?	Query the current pulse width in seconds.

QFNC(?){i} IQ Modulation Function

Set (query) the modulation function for IQ modulation {to i}. The parameter i may be set to one of the following values:

i	Modulation Function
4	Noise
5	External

Note: see MFNC, SFNC, and PFNC commands for AM/FM/ΦM, sweeps, and pulse/blank modulations respectively.

RATE(?){f}[u] Modulation Rate for AM/FM/ΦM

Set (query) the modulation rate for AM/FM/ΦM {to f}. If omitted, units default to Hz. This command also controls the noise bandwidth for AM/FM/ΦM and IQ modulation if a noise function is selected for the given type of modulation.

Note: use the SRAT command to control the sweep rates.

Example

RATE 400	Set the modulation rate to 400 Hz.
RATE 10 kHz	Set the rate to 10 kHz.
RATE?	Query the current rate in Hz.
RATE? kHz	Query the current rate in kHz.

RPER(?){t}[u] PRBS Period for Pulse/Blank Modulation

Set (query) the PRBS period for pulse/blank modulation{to t}. If omitted, units default to seconds. This value controls pulse modulation when the selected waveform is noise (see PFNC).

Example

RPER 1e-3	Set the bit period to 1 ms.
RPER?	Query the current bit period in seconds.

SDEV(?){f}[u] Sweep Deviation

Set (query) the deviation for sweeps {to f}. If omitted, units default to Hz. The limits for sweep deviations are controlled by the edges of the band within which the synthesizer is operating. Sweeps deviations may be as large as 1 GHz in the 2 to 4 GHz band.

Example

SDEV 100e6	Set the sweep deviation to 100 MHz.
SDEV?	Query the current sweep deviation in Hz.
SDEV 1 MHz	Set the sweep deviation to 1 MHz.

SFNC(?){i} Sweep Modulation Function

Set (query) the modulation function for sweeps {to i}. The parameter i may be set to one of the following values:

i	Modulation Function
0	Sine wave
1	Ramp
2	Triangle
5	External

Note: see MFNC, PFNC, and QFNC commands for AM/FM/ΦM, pulse/blank, and IQ modulations respectively.

SRAT(?){f}[u] Modulation Sweep Rate

Set (query) the modulation rate for sweeps {to f}. If omitted, units default to Hz.

Note: use the RATE command to control the modulation rate of AM/FM/ ΦM.

Example

SRAT 10	Set the sweep rate to 10 Hz.
SRAT?	Query the current rate in Hz.

TYPE(?){i} Modulation Type

Set (query) the current modulation type {to i}. The parameter i may be set to one of the following values:

i	Modulation Type
0	AM
1	FM
2	ΦM
3	Sweep
4	Pulse
5	Blank
6	IQ (if option 3 is installed)

Example

TYPE 2 Set the modulation type to phase modulation.

List Commands

For detailed information on creating and defining lists, see the section List Mode later in this chapter. Basic steps for using lists are summarized in Table 28.

Table 28: SG384 Basic List Configuration

Action	Relevant Commands
Create list	LSTC
Set instrument state for each list entry	LSTP
Enable list	LSTE
Trigger list	*TRG or GPIB bus trigger
Delete list	LSTD

All of these commands are described in detail below.

LSTC? i List Create

Create a list of size i. If successful, 1 is returned, otherwise 0 is returned. The list is initialized to the no change state.

Example

LSTC? 20 Create a list of size 20. Returns 1 if successful, otherwise 0.

LSTD List Delete

Delete the current list and free any memory dedicated to it.

Example

LSTD Destroy a previously created list.

LSTE(?){i} List Enable

Set (query) the list enable state {to i}. If i is 1, the list is enabled. If i is 0 it is disabled. A list must be enabled before it can be triggered.

Example

LSTE 1 Enable a previously created list.
LSTE? Query the current enable state of the list.

LSTI(?){i} List Index

Set (query) the current list index pointer {to i}.The list index identifies the entry whose state will be loaded into the instrument upon the next valid trigger.

Example

LSTI 10 Set the list index to 10.
LSTI? Query the current list index.

LSTP(?) i {,<st>} List Point

Set (query) the instrument state stored in entry i of the list {to <st>}. Details on the format and meaning of instrument states <st> are discussed above in the section List Instrument States.

Example

LSTP 5, 100e6,N,N,N,N,N,N,N,N,N,N,N,N,N
Set list entry 5 in the list to change the frequency to 100 MHz but leave all other settings unchanged.
LSTP? 5 Query instrument state stored in list entry 5.

LSTS? List Size

Query the current list size. This is the size requested when the list was created with the LSTC? command.

Interface Commands

EMAC? Ethernet MAC Address

Query the SG384's Ethernet MAC address.

EPHY(?){i} Ethernet Physical Layer Configuration

Set (query) the Ethernet link speed {to i}. The parameter i may be one of the following:

i	Link Speed
0	10 Base T
1	100 Base T

Example

EPHYS 1 Configure link for 100 Base T operation.

IFCF(?)i{,j} Interface Configuration

Set (query) interface configuration parameter i {to j}. The parameter i may be one of the following:

i	Configuration Parameter
0	RS-232 Enable/Disable
1	RS-232 Baud Rate
2	GPIB Enable/Disable
3	GPIB Address
4	LAN TCP/IP Enable/Disable.
5	DHCP Enable/Disable
6	Auto-IP Enable/Disable
7	Static IP Enable/Disable
8	Bare Socket Enable/Disable
9	Telnet Enable/Disable
10	VXI-11 Net Instrument Enable/Disable
11	Static IP Address
12	Subnet Address/Network Mask
13	Default Gateway

Set j to 0 to disable a setting and 1 to enable it. Valid RS-232 baud rates include 4800, 9600, 19200, 38400, 57600, and 115200. Valid GPIB addresses are in the range 0–30. Parameters 10–12 require an IP address in the form 'a.b.c.d' where each letter is a decimal integer in the range 0–255.

Example

IFCF 6,0	Disable Auto-IP
IFCF 1,19200	Set RS-232 baud rate to 19200
IFCF 3,16	Set primary GPIB address to 16
IFCF 11,192.168.10.5	Set IP address to 192.168.10.5
IFCF 12,255.255.255.0	Set network mask to 255.255.255.0
IFCF 13,192.168.10.1	Set default gateway to 192.168.10.1

IFRS i Interface Reset

Reset interface i. The parameter i identifies the interface to reset:

i	Interface
0	RS-232
1	GPIB
2	LAN TCP/IP

When an interface is reset all connections on that interface are reset to the power-on state.

IPCF? i Active TCP/IP Configuration

Query active TCP/IP configuration parameter i. The parameter i may be one of the following:

i	Configuration
0	Link
1	IP Address
2	Subnet Address/Network Mask
3	Default Gateway

The link parameter indicates whether the SG384 is physically connected to the LAN/Ethernet network. A value of 1 indicates the SG384 is connected. The rest of the parameters indicate the current TCP/IP configuration that was selected by the appropriate configuration process: DHCP, Auto-IP, or Static IP.

LCAL Go to Local

Go back to local control of the instrument. This enables the front panel key pad for instrument control. This command is only active on raw socket, telnet and RS-232 connections. The other interfaces have built in functionality for implementing this functionality.

LOCK? Request Lock

Request the instrument lock. The SG384 returns 1 if the lock is granted and 0 otherwise. When the lock is granted, no other instrument interface, including the front panel interface, may alter instrument settings until the lock is released via the UNLK command.

REMT Go to Remote

Enable remote control of the instrument. In this mode, the front panel key pad is disabled, so that control of the instrument can only occur via the remote interface. This command is only active on raw socket, telnet and RS-232 connections. The other interfaces have built in functionality for implementing this functionality.

UNLK? Release Lock

Release the instrument lock previously acquired by the LOCK? command. Returns 1 if the lock was released, otherwise 0.

XTRM i{,j,k} Interface Terminator

Set the interface terminator that is appended to each response to i, j, k.
The default terminator is 13, 10, which is a carriage return followed by a line feed.

Status Byte Definitions

The SG384 reports on its status by means of the serial poll status byte and two event status registers: the standard event status (*ESR) and the instrument event status (INSR). These read-only registers record the occurrence of defined events inside the SG384. If the event occurs, the corresponding bit is set to one. Bits in the status registers are latched. Once an event bit is set, subsequent state changes do not clear the bit. All bits are cleared when the registers are queried, with a *ESR?, for example. The bits are also cleared with the clear status command, *CLS. The bits are not cleared, however, with an instrument reset (*RST) or a device clear.

Each of the SG384's event status registers has an associated enable register. The enable registers control the reporting of events in the serial poll status byte (*STB). If a bit in the event status register is set and its corresponding bit in the enable register is set, then the summary bit in the serial poll status byte (*STB) will be set. The enable registers are readable and writable. Reading the enable registers or clearing the status registers does not clear the enable registers. Bits in the enable registers must be set or cleared explicitly. To set bits in the enable registers, write an integer value equal to the binary weighted sum of the bits you wish to set.

The serial poll status byte (*STB) also has an associated enable register called the service request enable register (*SRE). This register functions in a similar manner to the other enable registers, except that it controls the setting of the master summary bit (bit 6) of the serial poll status byte. It also controls whether the SG384 will issue a request for service on the GPIB bus.

Serial Poll Status Byte

Bit	Name	Meaning
0	INSB	An unmasked bit in the instrument status register (INSR) has been set.
1	Reserved	
2	Reserved	
3	Reserved	
4	MAV	The interface output buffer is non-empty
5	ESB	An unmasked bit in the standard event status register (*ESR) has been set.
6	MSS	Master summary bit. Indicates that the SG384 is requesting service because an unmasked bit in this register has been set.
7	Reserved	

The serial poll status byte may be queried with the *STB? command. The service request enable register (*SRE) may be used to control when the SG384 asserts the request-for-service line on the GPIB bus.

Standard Event Status Register

Bit	Name	Meaning
0	OPC	Operation complete. All previous commands have completed. See command *OPC.
1	Reserved	
2	QYE	Query error occurred.
3	DDE	Device dependent error occurred.
4	EXE	Execution error. A command failed to execute correctly because a parameter was invalid.
5	CME	Command error. The parser detected a syntax error.
6	Reserved	
7	PON	Power on. The SG384 has been power cycled.

The standard event status register may be queried with the *ESR? command. The standard event status enable register (*ESE) may be used to control the setting of the ESB summary bit in the serial poll status byte.

Instrument Status Register

Bit	Name	Meaning
0	20MHZ_UNLK	The 20 MHz PLL has come unlocked.
1	100MHZ_UNLK	The 100 MHz PLL has come unlocked.
2	19MHZ_UNLK	The 19 MHz PLL has come unlocked.
3	1GHZ_UNLK	The 1 GHz PLL has come unlocked.
4	4GHZ_UNLK	The 4 GHz PLL has come unlocked.
5	NO_TIMEBASE	An installed optional timebase is not oscillating.
6	RB_UNLK	An installed Rubidium timebase is unlocked.
7	Reserved	
8	MOD_OVLD	An external modulation overload was detected.
9	IQ_OVLD	An external IQ modulation overload was detected.
10-15	Reserved	

The instrument status register may be queried with the INSR? command. The instrument status enable register (INSE) may be used to control the setting of the INSB summary bit in the serial poll status byte.

List Mode

The SG384 supports a powerful list mode, only available via the remote interface, which enables the user to store a list of instrument states in memory and quickly switch between states by sending GPIB bus triggers or the *TRG command.

List Instrument States

At the heart of the list configuration is the instrument state which should be loaded upon the reception of each valid trigger. The instrument state is downloaded to the SG384 via the command: LSTP i {, <st>}. The parameter i is the index identifying the list entry to which the instrument state, <st>, should be stored. The instrument state, <st>, consists of an ordered, comma-separated list of 15 values. The order and description of each value is summarized in Table 29.

Also listed in the table are related, non-list, commands that also change the given instrument state. For example, frequency is the first parameter. Entering a value here would change the carrier frequency to the given value just as the FREQ command would do.

The parameter for each state is set with a floating point value or integer in the default units as specified by the related commands. For example, entering a 100e6 in the first position would set the frequency to 100 MHz.

Although, all parameters in <st> must be specified, each parameter may be specified as 'N' to leave the parameter unchanged. Thus, to leave all parameters unchanged, set the state as follows:

<All unchanged> = N,N,N,N,N,N,N,N,N,N,N,N,N,N,N

This is the default for all entries when a list is created. To change just one item, simply specify that one item and leave all others unchanged. For example, to only change the BNC output amplitude use the following state:

<BNC ampl: –2 dBm> = N,N,-2.00,N,N,N,N,N,N,N,N,N,N,N,N

Performing scans of frequency or amplitude consists of storing successive instrument list states in which only the frequency is changed, or only the amplitude is changed, respectively. To scan frequency and amplitude simultaneously, simply specify both frequency and amplitude for each state. For example, to change the frequency to 100 MHz and the BNC output to –2 dBm use the following state:

<Freq. and BNC ampl> = 100e6,N,-2.00,N,N,N,N,N,N,N,N,N,N,N,N

If a given setting happens to be invalid when the triggered state occurs, the parameter will be ignored. This might happen, for instance, if one tries to enable pulse modulation with the frequency set to 5 GHz.

Table 29: SG384 List State Definitions

Position	Instrument State	Related Commands
1	Frequency	FREQ
2	Phase	PHAS
3	Amplitude of LF (BNC output)	AMPL
4	Offset of LF (BNC output)	OFSL
5	Amplitude of RF (N-type output)	AMPR
6	Front panel display	DISP
7	Enables/Disables	
	Bit 0: Enable modulation	MODL
	Bit 1: Disable LF (BNC output)	ENBL
	Bit 2: Disable RF (N-type output)	ENBR
	Bit 3: Disable Clock output	ENBC
	Bit 4: Disable HF (RF doubler output)	ENBH
8	Modulation type	TYPE
9	Modulation function	
	AM/FM/ ΦM	MFNC
	Sweep	SFNC
	Pulse/Blank	PFNC
	IQ	QFNC
10	Modulation rate	
	AM/FM/ΦM modulation rate	RATE
	Sweep rate	SRAT
	Pulse/Blank period	PPER, RPER
11	Modulation deviation	
	AM	ADEP, ANDP
	FM	FDEV, FNDV
	ΦM	PDEV, PNDV
	Sweep	SDEV
	Pulse/Blank	PWID
12	Amplitude of clock output	AMPC
13	Offset of clock output	OFSC
14	Amplitude of HF (RF doubler output)	AMPH
15	Offset of rear DC	OFSD

Enables/Disables

The enables/disables setting at position 7 in the state list is different from the others in that multiple commands are aggregated into one value and the polarities of the disables are opposite to that of their corresponding commands. Modulation enable is assigned to bit 0. The output disables are assigned to bits 1 to 4. The enable/disables value is then calculated as the binary weighted sum of all the bits.

For example, to enable modulation and disable the clock and RF doubler outputs, we need to set bits 0, 3, and 4. The binary weighted sum is given as $2^0 + 2^3 + 2^4 = 1 + 8 + 16 = 25$. Thus, a value of 25 in position 7 would enable the modulation and disable the clock and RF doubler outputs.

Modulation List States

Virtually all modulation parameters may be specified as part of a list state, but not simultaneously. In order to compress the size of the list, many parameters share the same position as indicated in Table 19. Thus, in order to untangle which parameters are being specified, the modulation type must be specified. Furthermore, if modulation rate or deviation is specified, then both the modulation type and modulation function must also be specified.

For example, to set AM sine wave modulation depth to 25 %, specify the list state as follows:

<Mod AM: 25%> = N,N,N,N,N,N,N,0,0,N,25.0,N,N,N,N

Similarly, to set FM sine wave modulation deviation to 100 kHz, specify the list state as follows:

<Mod FM: 100 kHz> = N,N,N,N,N,N,N,1,0,N,100e3,N,N,N,N

Specify a frequency sweep of 100 MHz at a 10 Hz rate with a 750 MHz carrier and modulation enabled as follows:

<Sweep: 100 MHz at 10 Hz> = 750e6,N,N,N,N,N,1,3,1,10.0,100e6,N,N,N,N

Specify pulse modulation with a 1 ms period and 10 μs width as follows:

<Mod pulse: 1 ms period, 10 μs width> = N,N,N,N,N,N,N,4,3,1e-3,10e-6,N,N,N,N

Note that although the modulation type and modulation function must usually be specified together, the modulation itself need not necessarily be enabled. Thus, one could configure the modulation in one list entry and enable it in another entry.

Examples

Example 1: Scan frequency from 100 MHz to 1 GHz in 100 MHz steps.

```
LSTC? 10
LSTP 0,100e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 1,200e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 2,300e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 3,400e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 4,500e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 5,600e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 6,700e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 7,800e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 8,900e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTP 9,1000e6,N,N,N,N,N,N,N,N,N,N,N,N,N,N
LSTE 1
```

Example 2: Scan RF N-type output from 10 dBm to -10 dBm in 5 dBm steps.

```
LSTC? 5
LSTP 0,N,N,N,N,10.0,N,N,N,N,N,N,N,N,N,N
LSTP 1,N,N,N,N,5.0,N,N,N,N,N,N,N,N,N,N
LSTP 2,N,N,N,N,0.0,N,N,N,N,N,N,N,N,N,N
LSTP 3,N,N,N,N,-5.0,N,N,N,N,N,N,N,N,N,N
LSTP 4,N,N,N,N,-10.0,N,N,N,N,N,N,N,N,N,N
LSTE 1
```

Example 3: Configure pulse modulation with 1 ms period and scan the width from 100 μs to 900 μs in 100 μs steps.

```
LSTC? 9
LSTP 0,N,N,N,N,N,N,1,4,3,1e-3,100e-6,N,N,N,N
LSTP 1,N,N,N,N,N,N,N,4,3,N,200e-6,N,N,N,N
LSTP 2,N,N,N,N,N,N,N,4,3,N,300e-6,N,N,N,N
LSTP 3,N,N,N,N,N,N,N,4,3,N,400e-6,N,N,N,N
LSTP 4,N,N,N,N,N,N,N,4,3,N,500e-6,N,N,N,N
LSTP 5,N,N,N,N,N,N,N,4,3,N,600e-6,N,N,N,N
LSTP 6,N,N,N,N,N,N,N,4,3,N,700e-6,N,N,N,N
LSTP 7,N,N,N,N,N,N,N,4,3,N,800e-6,N,N,N,N
LSTP 8,N,N,N,N,N,N,N,4,3,N,900e-6,N,N,N,N
LSTE 1
```

Example 4: Configure AM modulation at1 kHz rate and scan the depth from 25 % to 100 % in 25 % steps.

```
LSTC? 4
LSTP 0,N,N,N,N,N,N,1,0,0,1e3,25,N,N,N,N
LSTP 1,N,N,N,N,N,N,N,0,0,N,50,N,N,N,N
LSTP 2,N,N,N,N,N,N,N,0,0,N,75,N,N,N,N
LSTP 3,N,N,N,N,N,N,N,0,0,N,100,N,N,N,N
LSTE 1
```

Error Codes

The SG384 contains an error buffer that may store up to 20 error codes associated with errors encountered during power-on self tests, command parsing, or command execution. The ERR LED will be highlighted when a remote command fails for any reason. The errors in the buffer may be read one by one by executing successive LERR? commands. The user may also view the errors from the front panel by pressing the keys [SHIFT], 'STATUS', sequentially, followed by ADJUST △ until the display reads 'Error Status.' Finally, press SELECT ▷ successively to view the error count and individual errors. The errors are displayed in the order in which they occurred. The ERR LED will go off when all errors have been retrieved.

The meaning of each of the error codes is described below.

Execution Errors

0 No Error

No more errors left in the queue.

10 Illegal Value

A parameter was out of range.

11 Illegal Mode

The action is illegal in the current mode. This might happen, for instance, if the user tries to turn on IQ modulation with the 'MODL 1' command and the current frequency is below 400 MHz.

12 Not Allowed

The requested action is not allowed because the instrument is locked by another interface.

13 Recall Failed

The recall of instrument settings from nonvolatile storage failed. The instrument settings were invalid.

14 No Clock Option

The requested action failed because the rear clock option is not installed.

15 No RF Doubler Option

The requested action failed because the rear RF doubler option is not installed.

16 No IQ Option

The requested action failed because the rear IQ option is not installed.

17 Failed Self Test

This value is returned by the *TST? command when the self test fails.

Query Errors

30 Lost Data

Data in the output buffer was lost. This occurs if the output buffer overflows or if a communications error occurs and data in output buffer is discarded.

32 No Listener

This is a communications error that occurs if the SG384 is addressed to talk on the GPIB bus, but there are no listeners. The SG384 discards any pending output.

Device Dependent Errors

40 Failed ROM Check

The ROM checksum failed. The firmware code is likely corrupted.

42 Failed EEPROM Check

The test of EEPROM failed.

43 Failed FPGA Check

The test of the FPGA failed.

44 Failed SRAM Check

The test of the SRAM failed.

45 Failed GPIB Check

The test of GPIB communications failed.

46 Failed LF DDS Check

The test of the LF DDS communications failed.

47 Failed RF DDS Check

The test of the RF DDS communications failed.

48 Failed 20 MHz PLL

The test of the 20 MHz PLL failed.

49 Failed 100 MHz PLL

The test of the 100 MHz PLL failed.

50 Failed 19 MHz PLL

The test of the 19 MHz PLL failed.

51 Failed 1 GHz PLL

The test of the 1 GHz PLL failed.

52 Failed 4 GHz PLL

The test of the 4 GHz PLL failed.

53 Failed DAC

The test of the internal DACs failed.

Parsing Errors

110 Illegal Command

The command syntax used was illegal. A command is normally a sequence of four letters, or a '*' followed by three letters.

111 Undefined Command

The specified command does not exist.

112 Illegal Query

The specified command does not permit queries

113 Illegal Set

The specified command can only be queried.

114 Null Parameter

The parser detected an empty parameter.

115 Extra Parameters

The parser detected more parameters than allowed by the command.

116 Missing Parameters

The parser detected missing parameters required by the command.

117 Parameter Overflow

The buffer for storing parameter values overflowed. This probably indicates a syntax error.

118 Invalid Floating Point Number

The parser expected a floating point number, but was unable to parse it.

120 Invalid Integer

The parser expected an integer, but was unable to parse it.

121 Integer Overflow

A parsed integer was too large to store correctly.

122 Invalid Hexadecimal

The parser expected hexadecimal characters but was unable to parse them.

126 Syntax Error

The parser detected a syntax error in the command.

127 Illegal Units

The units supplied with the command are not allowed.

128 Missing Units

The units required to execute the command were missing.

Communication Errors

170 Communication Error

A communication error was detected. This is reported if the hardware detects a framing, or parity error in the data stream.

171 Over run

The input buffer of the remote interface overflowed. All data in both the input and output buffers will be flushed.

Other Errors

254 Too Many Errors

The error buffer is full. Subsequent errors have been dropped.

Example Programming Code

The following program can be used as sample code for communicating with the SG384 over TCP/IP. The program is written in the C++ language and should compile correctly on a Windows based computer. It could be made to work on other platforms with minor modifications. In order to use the program, you will need to connect the SG384 to your LAN and configure it with an appropriate IP address. Contact your network administrator for details on how to do this. To identify the SG384's current IP address from the front panel press [SHIFT], [STATUS], then repeat press △until the 'tcp ip status' menu appears. Finally press the [◁] [▷] to sequence to the 'ip' address.

Copy the program into a file named "sg_ctrl.cpp". To avoid typing in the program manually, download the electronic version of this manual from the SRS website (www.thinksrs.com). Select the program text and copy/paste it into the text editor of your choice. Compile the program into the executable "sg_ctrl.exe". At the command line type something like the following:

```
sg_ctrl 192.168.0.5
```

where you will replace "192.168.0.5" with the IP address of the SG384. You should see the something like the following:

```
Connection Succeeded

Stanford Research Systems,SG384,s/n001013,ver1.00.10A

Closed connection
```

The program connects to the SG384 at the supplied IP address sets several parameters and then closes. If successful, the frequency should be set to 50 MHz and the amplitudes of N-Type and BNC outputs will be set to -10 and -5 dBm, respectively.

```c
/* sg_ctrl.c : Sample program for controlling the SG384 via TCP/IP */
#include "Winsock2.h"
#include <stdio.h>

/* prototypes */
void init_tcpip(void);
int sg_connect(unsigned long ip);
int sg_close(void);
int sg_write(char *str);
int sg_write_bytes(const void *data, unsigned num);
int sg_read(char *buffer, unsigned num);

SOCKET sSG384;               /* sg384 tcpip socket */
unsigned sg_timeout = 6000;  /* Read timeout in milliseconds */

int main(int argc, char * argv[])
{
  char buffer[1024];

  /* Make sure ip address is supplied on the command line */
  if ( argc < 2 ) {
    printf("Usage: sg_ctrl IP_ADDRESS\n");
    exit(1);
  }

  /* Initialize the sockets library */
  init_tcpip();

  /* Connect to the sg384 */
  if ( sg_connect( inet_addr(argv[1]) ) ) {
    printf("Connection Succeeded\n");

    /* Get identification string */
    sg_write("*idn?\n");
    if ( sg_read(buffer,sizeof(buffer)) )
      printf(buffer);
    else
      printf("Timeout\n");
    /* Reset instrument */
    sg_write("*rst\n");
    /* Set frequency to 50 MHz */
    sg_write("freq 50e6\n");
    /* Set amplitude of N-type output to -10 dBm */
    sg_write("ampr -10.0\n");
    /* Set amplitude of BNC output to -5 dBm */
    sg_write("ampl -5.0\n");
    /* Make sure all commands have executed before closing connection */
    sg_write("*opc?\n");
    if ( !sg_read(buffer,sizeof(buffer)) )
      printf("Timeout\n");
    /* Close the connection */
    if (sg_close())
      printf("Closed connection\n");
    else
      printf("Unable to close connection");
  }
  else
    printf("Connection Failed\n");

      return 0;
}
```

```
void init_tcpip(void)
{
  WSADATA wsadata;
  if ( WSAStartup(2, &wsadata) != 0 ) {
    printf("Unable to load windows socket library\n");
    exit(1);
  }
}

int sg_connect(unsigned long ip)
{
  /* Connect to the sg384 */
  struct sockaddr_in intrAddr;
  int status;

  sSG384 = socket(AF_INET,SOCK_STREAM,0);
  if ( sSG384 == INVALID_SOCKET )
    return 0;

  /* Bind to a local port */
  memset(&intrAddr,0,sizeof(intrAddr));
  intrAddr.sin_family = AF_INET;
  intrAddr.sin_port = htons(0);
  intrAddr.sin_addr.S_un.S_addr = htonl(INADDR_ANY);
  if ( SOCKET_ERROR == bind(sSG384,(const struct sockaddr
*)&intrAddr,sizeof(intrAddr)) ) {
    closesocket(sSG384);
    sSG384 = INVALID_SOCKET;
    return 0;
  }

  /* Setup address for the connection to dg on port 5025 */
  memset(&intrAddr,0,sizeof(intrAddr));
  intrAddr.sin_family = AF_INET;
  intrAddr.sin_port = htons(5025);
  intrAddr.sin_addr.S_un.S_addr = ip;
  status = connect(sSG384,(const struct sockaddr *)&intrAddr,sizeof(intrAddr));
  if ( status ) {
    closesocket(sSG384);
    sSG384 = INVALID_SOCKET;
    return 0;
  }
  return 1;
}

int sg_close(void)
{
  if ( closesocket(sSG384) != SOCKET_ERROR )
    return 1;
  else
    return 0;
}

int sg_write(char *str)
{
  /* Write string to connection */
  int result;

  result = send(sSG384,str,(int)strlen(str),0);
  if ( SOCKET_ERROR == result )
    result = 0;
  return result;
}
```

```
int sg_write_bytes(const void *data, unsigned num)
{
  /* Write string to connection */
  int result;

  result = send(sSG384,(const char *)data,(int)num,0);
  if ( SOCKET_ERROR == result )
    result = 0;
  return result;
}

int sg_read(char *buffer, unsigned num)
{
  /* Read up to num bytes from connection */
  int count;
  fd_set setRead, setWrite, setExcept;
  TIMEVAL tm;

  /* Use select() so we can timeout gracefully */
  tm.tv_sec = sg_timeout/1000;
  tm.tv_usec = (sg_timeout % 1000) * 1000;

  FD_ZERO(&setRead);
  FD_ZERO(&setWrite);
  FD_ZERO(&setExcept);
  FD_SET(sSG384,&setRead);
  count = select(0,&setRead,&setWrite,&setExcept,&tm);
  if ( count == SOCKET_ERROR ) {
    printf("select failed: connection aborted\n");
    closesocket(sSG384);
    exit(1);
  }
  count = 0;
  if ( FD_ISSET(sSG384,&setRead) ) {
    /* We've received something */
    count = (int)recv(sSG384,buffer,num-1,0);
    if ( SOCKET_ERROR == count ) {
      printf("Receive failed: connection aborted\n");
      closesocket(sSG384);
      exit(1);
    }
    else if (count ) {
      buffer[count] = '\0';
    }
    else {
      printf("Connection closed by remote host\n");
      closesocket(sSG384);
      exit(1);
    }
  }
  return count;
}
```

Circuit Description

Overview

The SG384 is a dc-4.05 GHz signal generator with extensive modulation capabilities. The unit's low phase noise (–110 dBc/Hz at 20 kHz offset at 1 GHz) and high resolution (1 µHz at all frequencies) are provided by a unique synthesis technique that allows essentially zero channel spacing together with a high phase comparison frequency without the noise or spurs associated with conventional fractional-N synthesis.

Several options improve or extend the performance of the SG384. Option 1 provides complimentary clock outputs with 35 ps transition times. Option 2 is a frequency doubler that provides a rear panel SMA output up to 8.1 GHz. Option 3 provides high bandwidth rear panel I/Q modulation inputs. Option 4 improves the timebase accuracy with a rubidium oscillator.

Block Diagram

(Schematic 1: Block Diagram)

Important sections of the instrument, and the interconnections between them, are illustrated in the block diagram. We will follow the RF signal path first, and then we will discuss the various support functions.

The RF path starts in the upper left corner with the Timebase and ends in the lower right corner with the Output Amplifiers and Attenuators. The Timebase consists of a 20 MHz VCXO that is phase locked to an internal OCXO, to an internal rubidium Timebase (Option 4), or to an external 10 MHz reference. A 100 MHz VCXO is phase locked to the 20 MHz Timebase. The 100 MHz is divided by four to provide 25 MHz to the CPU and FPGA. The 100 MHz is also the sample clock for a 48-bit DDS (here after referred to as the LF DDS). The frequency resolution of the LF DDS is extended to 64 bits via the FSK pin of the LF DDS. The output frequency of the instrument is proportional to the frequency output of this LF DDS and so this establishes the instrument's frequency resolution.

The output of the LF DDS cannot serve directly as the reference for the RF synthesizer because spurs on the LF DDS output would appear on the RF output, increased in magnitude by 6 dB per octave between the LF DDS output and the instrument's RF output. Hence, one of three VCXOs is used to filter the LF DDS output to remove the spurs. Two of the VCXOs can be tuned by ±100 ppm (around 19.5541 MHz or 19.6617 MHz), while the third VCXO can be tuned by ±10 ppm around 19.607843 MHz (collectively referred to hereafter as 19+ MHz VCXO). These frequencies were chosen to maximize the phase comparison frequency in the RF synthesizer's PLL, as well as optimizing performance at canonical frequencies. The LF DDS is programmed to operate in one of these three ranges and the corresponding VCXO is phase locked to the LF DDS. The output of the phase locked VCXO, whose frequency can now be set with 64 bits of resolution, becomes the timebase for the RF synthesizer.

The selected 19+ MHz VCXO is multiplied up by ×51 to a frequency near 1 GHz by the PLL synthesizer in the "RF Reference / Baseband DDS" section of the block diagram. The 1 GHz output serves as the sample clock to a 32-bit DDS (hereafter referred to as the RFDDS). The output of the RFDDS becomes the reference frequency for the RF synthesizer. The RFDDS is programmed to divide by an integer when it is used as a reference for an unmodulated RF output. Dividing by an integer eliminates DDS spurs, as the DDS repeats the exact same sequence for every cycle of its divided output and so "spurs" collect together as harmonics which do not cause clock jitter or spurious frequency outputs (refer to Appendix A). When generating frequency or phase modulated outputs the RFDDS provides agile modulation of the RF reference frequency via the 16-bit words from the FPGA modulation processor, which are updated at 125 MHz.

The output of the 1 GHz, 32-bit, RFDDS is filtered and passed differentially to the RF synthesizer in the RF Block to serve as the PLL frequency reference, f_{ref} . A wideband VCO (1900-4100 MHz) is divided by N and phase locked to the reference divided by R, to produce and output frequency of $f_{ref} \times N / R$. The output of this synthesizer clocks binary dividers to provide square wave outputs between 59.375 MHz and 4100 MHz. The square waves are low-pass filtered to provide sine wave outputs over the same frequency range. An RF multiplexer selects one of the sine waves, or the original reference sine wave in the case that the RF output is less than 62.5 MHz, as the source to the RF output stages. Another RF multiplexer selects the corresponding square wave to serve as the source for the rear panel clock and doubler options.

The selected RF sine wave is passed to the RF "Output amplifiers and attenuators" block. An I/Q modulator is inserted into the signal path when I/Q modulation is being used, otherwise the RF output is passed directly to a series of RF attenuators and amplifiers which provide an output amplitude range from –107 dBm to +13 dBm. A voltage variable attenuator is used to provide amplitude modulation. The amplified and attenuated RF sine wave, in the frequency range of 950 kHz to 4.05 GHz, is output via the front panel type-N connector.

There is another signal path for output signals between dc and 62.5 MHz. The 32-bit RFDDS on the mother board provides signals in this range directly. The differential signals are passed to the output block and can be amplified or attenuated to a range from $1mV^{rms}$ to $1V_{rms}$ and offset with a dc voltage. The amplified and offset output is passed out the front panel BNC connector via 50 Ω.

There are several modulation paths. As previously described, frequency and phase modulation is provided by the FPGA via the RFDDS's parallel port. The source for the modulation waveform can be a table in the FPGA, data stored in a larger memory external to the FPGA, or up-sampled and digitally filtered data streaming from an ADC which digitizes the rear panel modulation input. An analog copy of the modulation waveform is output via a rear panel BNC.

Analog signals to provide I/Q modulation can originate from table in the FPGA, or data stored in a larger memory external to the FPGA, up-sampled to 125 MHz, digitally filtered, and output via dual 14-bit DACs. I/Q modulation can also be provided directly via rear panel BNC inputs (Option 3). Copies of the I&Q modulation waveforms can be output via rear panel BNCs (Option 3).

Amplitude modulation can originate from a table in the FPGA, data stored in a larger memory external to the FPGA, or up-sampled data streaming from an ADC which

digitizes the rear panel modulation input. RF outputs above 62.5 MHz are amplitude modulated via a voltage variable attenuator in the RF output stages. Outputs below 62.5 MHz are amplitude modulated via the 16-bit parallel port on the RFDDs. An analog of the modulation waveform is output via a rear panel BNC.

A Coldfire™ microcontroller is used to control all aspects of the instrument's operation and to interface to external computers via the Ethernet, GPIB or RS-232. The microcontroller also responds to front panel key presses and updates front panel displays.

The front panel display is fully static (there is one latched bit per display segment or indicator lamp.) This approach eliminates the possibility of a display refresh spur in the RF output. The front panel display is written to and read from serially when a change is made or a key is pressed.

The system power supply is enclosed in a separate enclosure within the instrument for safety and shielding. A universal input power supply converts the line voltage to +24 V_{DC} which is always present to provide power to the OCXO or optional rubidium timebase. An inverter operates to provide $\pm$15, $\pm$5, and +3.3 V when the unit is switched "on" to power the rest of the instrument.

Detailed Circuit Description

Several sub-assemblies will be described:

1. The front panel display
2. The front panel display Shield
3. The mother board
4. The RF synthesizer
5. The RF output amplifiers and attenuators
6. The power supply
7. Option 1 (high speed clock outputs)
8. Option 2 (4-8 GHz RF output)
9. Option 3 (I/Q modulation inputs & outputs)
10. Option 4 (Rubidium Timebase)

Front-Panel Display

(Schematic 2: Front Panel Display)

The front panel consists of 16 seven-segment displays, 47 LED lamps, and 33 key conductive rubber keypads. The front panel display is fully static in that there is one latched bit for each LED segment or lamp. Data is written to the display serially via the SPI (Serial Peripheral Interface Bus). When a key is pressed, the input to the corresponding latch is pulled high, and a KEYPRESS interrupt is sent to the CPU. Key press data is latched when the CPU responds with a –CS_FRONT. As data is being written to the display, latched key press data is also read back over the SPI.

The lamp currents (which set brightness) are equal to the +3.3 V supply, minus the ≈2 V LED voltage, divided by resistance of the current limiting network (100 Ω). The LED display segment current (which sets segment brightness) is equal to +3.3 V supply, minus the≈1.5 V LED voltage, minus the 0.7 V base-emitter voltage of Q1A (for example), divided by resistance of the current limiting network (680 Ω). The intensity of a digit can be increased by turning on the other transistor in the pair (Q1B, for example) by setting Q7 of U43 low and asserting –INTENSIFY, which will cause the voltage on the common anode of U16 to increase by about 0.6 V.

Front-Panel Display Shield

(Schematic 3: Display EMI Filter)

The Front panel Display is shielded from the main box (via a metal chassis). The SPI interface and power connections are filtered by a separate PCB . These help to eliminate EMI and reduce the display interference in the main system's sensitive electronic.

Motherboard

The motherboard is the large PCB nearest to and approximately the same size as the bottom cover of the instrument. There are eight pages of schematics for the motherboard. Circuits include 10 MHz & 20 MHz timebases, three 19+ MHz VCXOs, Coldfire CPU with Ethernet, GPIB, and RS-232 interfaces, FPGA modulation processor, modulation DACs and external modulation ADC, 1 GHz VCO, an RF reference DDS, and interfaces to the RF Block and the rear panel options.

Timebases

(Schematic 4: Mother Board 1, Frequency Refs)

The timebase reference is a 20 MHz VCXO consisting of the 3rd overtone crystal, Y100, and the Colpitts oscillator, Q100. The crystal is designed to operate with a 20 pF load which is the series combination of C110, the tank L103/C111, and the varactor D100. To provide gain, both C110 and the parallel combination of L103 & C111 must have a capacitive reactance. The L103/C111 tank has an inductive reactance below 8.9 MHz which prevents the oscillator from operating at the fundamental frequency of the crystal. The crystal is operated just above its series resonance, and so has an inductive reactance that resonates with the load capacitance. The operating frequency is controlled by the dc voltage applied to the varactor.

The oscillator's circulating current is cascoded into the emitter of Q101 through to the collector, which is held at dc ground by L105 and amplitude limited by the dual Schottky, U105. The output is amplified and buffered by the low noise amplifier, U107, which provides a (nearly) square wave output with amplitude of about 2.4 Vpp at 20 MHz. This signal is ac coupled and converted to a 3.3 V CMOS level square wave by U114, which is powered by a low noise source, U112.

The 20 MHz square wave can be phase locked to an external timebase reference or to an internal OCXO or optional rubidium oscillator by the PLL synthesizer, U106. The 10 MHz RF input to the PLL synthesizer is selected by the multiplexer U109. Another multiplexer, U103, improves isolation between the internal OCXO or rubidium reference and the external timebase reference.

The presence of an internal reference is detected by the diodes U100 and the corresponding peak detection circuit. The presence of an external reference is detected by the diodes U104 and the corresponding peak detection circuit. The CPU operates the multiplexers to select the external reference whenever it is available, the internal OCXO or rubidium next, or a fixed programming voltage to adjust the 20 MHz VCXO as a last resort.

The PLL synthesizer's charge pump output is conditioned by the loop filter U110B. The loop filter has a bandwidth of about 140 Hz. The multiplexer U108 selects between the charge pump output (when the PLL is active) or a fixed programming voltage, CAL_VCO (when no better reference is available). A lock detect signal is provided to the CPU.

The 20 MHz is divided by two by U115, which drives transformer T100 differentially. The output of the transformer is low pass filtered (with a notch at 30 MHz) to provide the 10 MHz sine wave timebase output on a rear panel BNC.

A 100 MHz VCXO, U119, is phase locked to the 20 MHz reference by U116, a CMOS PLL frequency synthesizer. The differential outputs from the VCXO are used to clock a 48-bit DDS, and converted to CMOS logic levels and divided by 4 to generate 25 MHz clocks for the CPU and FPGA sections.

LF DDS and 19 MHz Reference

(Schematic 5: Mother Board 2, 19 MHz Ref)

The singular purpose of this page of schematics is to produce a low noise "19MHZ_REF" square wave which serves as the reference frequency for the rest of the RF synthesizer chain. A DDS (hereafter referred to as the LF DDS) is used to provide a frequency reference of 19 MHz and a resolution of $1{:}10^{18}$. Spurs and noise outside of the PLL loop bandwidth are rejected from the DDS output by phase locking a narrowband VCXO to the LF DDS. Spurs at all frequencies are reduced by applying a PRBS (pseudo-random binary sequence) to the FSK (frequency-shift key) input of the LF DDS with a repetition rate of about 98 kHz.

There are three nearly identical VCXOs. Each uses a crystal resonator in a Colpitts oscillator. The middle VCXO (19.607843 MHz) uses a 3rd overtone crystal and so has less phase noise and a narrower tuning range than the other VCXOs. The configuration of the middle VCXO is identical to the 20 MHz timebase described above. The circulating oscillator current is cascoded into the emitter of Q204. The collector load (L204 and back-to-back Schottky diodes U204) shape the signal current into a nearly square wave with no dc offset.

One of the three VCXOs is selected to be phase locked to the LF DDS. The selected VCXO has its output amplifier (U209, U210 or U211) enabled. An output multiplexer (U206, U207 or U208) connects the selected VCXO output to the input of U213, which shapes the selected signal into a CMOS level square wave.

The 100 MHz timebase serves as the clock to a LF DDS (U215) which is programmed to generate frequencies over three ranges: 19.5541 MHz$\pm$100ppm, 19.607843 MHz $\pm$10 ppm and 19.6617 MHz $\pm$100 ppm. The frequency resolution of the 48-bit LF DDS is extended to 64-bits by toggling between two frequency tuning words with a duty cycle that has 16 bits of resolution. The differential output of the LF DDS is transformer coupled to a low pass filter (L217-222 and C252-254) that has a cutoff frequency of 24 MHz.

Spurs and broadband noise are rejected from the output of the LF DDS by phase locking one of three VCXOs to the LF DDS output. The selected VCXO is phase locked by a CMOS PLL synthesizer, U217. One of two loop filters is used: U216A, a loop filter with 1.5 kHz bandwidth, is used when the selected VCXO is one of the fundamental mode oscillators. U216B, a loop filter with 150 Hz bandwidth, is used when the 3rd overtone oscillator is selected.

Microcontroller and Interface

(Schematic 6: Mother Board 3, CPU)

A Coldfire™ MCF52235 microcontroller is used to control the instrument and to interface to external computers via Ethernet, GPIB or RS-232. The microcontroller uses a 32-bit data path, has 256k of program flash ROM, 32k of RAM, an octal 12-bit ADC, and operates at 60 MHz from a 25 MHz clock input.

The microcontroller's ADCs are used to detect various PLL lock states, detect 10 MHz references, measure the control voltages applied to various VCOs, sense RF block temperature, measure the detected RF output, and measure miscellaneous systems voltages.

One of the microcontroller's UARTs is translated to RS-232 levels by U311 and made available on the rear panel for control by remote computers. The microcontroller's Ethernet controller is connected directly to a RJ-45 connector, U302, which is accessible on the rear panel to connect the instrument to a local area network. An 8-bit bidirectional port is used to interface the microcontroller to a GPIB controller, U316, whose connector is also on the instrument's rear panel.

The microcontroller's SPI (serial peripheral interface bus) is expanded to 16 ports by the decoders U308 and U309. The eight devices which are selected by U309 (PLL synthesizers, RF and Option control) are designated as "quiet" SPI devices. The SPI data and clock signals are only presented to these devices when one in the group is being addressed. Doing so reduces crosstalk disturbances which can add spurs to RF outputs. The AND gates in U312 gate "off" the QSCK and QMOSI signals unless the U309 decoder is enabled.

SPI devices include:

0) Idle, 1) spare, 2) FPGA modulation processor, 3) 19 MHz DDS, 4) RF DDS, 5) cal ROM flash, 6) front panel display, 7) miscellaneous control bits, 8) 20 MHz PLL, 9) 100 MHz PLL, 10) 19 MHz PLL, 11) 1 GHz PLL, 12) 4 GHz PLL, 13) RF block control, 14) Option 1&2 control, 15) system DAC.

Modulation Processor

(Schematic 7: Mother Board 4, Modulation Processor)

A Xilinx XC3S400A in a 320-pin BGA is used as a modulation processor in the SG384. The FPGA is attached to two large memories via a 16-bit data bus. The E28F320J3D75A, U402, is a Numonyx 32 MBit flash MEMORY which is used to store FPGA configurations and user arbitrary waveforms. The CY62167DV30, U400, is a Cypress 16 MBit, 55 ns static RAM used to store and play modulation waveforms.

Several FPGA configurations are stored in the flash MEMORY. Each configuration allows the FPGA to perform a variety of modulation tasks depending on the instrument configuration. For example, when EXT FM is selected, the FPGA reads digitized data from the ADC (U502) which digitizes the rear panel modulation input, then offsets, scales, and up-samples that data, and applies the result to the RF DDS's (U605) parallel input to frequency modulate the RF synthesizer's frequency reference. Another example: When the instrument is set to provide a wide span frequency ramp (Sweep, triangle, with a set modulation rate and modulation deviation) the FPGA is configured as a DDS to provide addresses that walk though a ramp of frequency values at a precise rate and provides interpolated frequency values to the parallel input of the RF DDS (U605). The FPGA will also control the values on the data bus LVL_DAC[0..13] which controls the analog signals ±RF_ATTN so as to level the amplitude of the RF output during the frequency sweep. A final example (this is a hardware provision for a future product): A user provided I/Q modulation pattern can be loaded into the static RAM. Data pairs are read from the RAM at a precise symbol rate, interpolated and up-sampled to about 125 MSPS, digitally filtered (by a root-raised cosine filter, for example), and the result applied to the dual 14-bit DAC (U513). The analog outputs from the dual DAC are filtered and applied differentially to the I/Q modulator in the RF block.

The FPGA has three clock sources whose use depends on the FPGA configuration. The PDCLK (which originates at RF DSS, U605, operating at the RF DDS frequency/4 or about 250 MHz) is used whenever the FPGA provides data to the RF DDS's parallel port. Timing is very critical in this case. The parallel data to the FPGA must arrive within a ±1 ns window with respect to the PDCLK. One of the FPGA's DCMs (Digital Clock Managers) is used to adjust the phase of the parallel output data to meet this timing requirement. The FPGA is able to measure the timing relationship between the PDCLK and the LSB of the parallel data (MD0) via IP_L32N and IP_L32P (at the upper right-hand corner of U401 on sheet 4 of 8.

The SYNC_CLK is used as the FPGA clock source when the FPGA is controlling the modulation via the profile inputs on the RF DDS (U605). Changes to the profile pins must arrive within a ±1 ns window with respect to the SYNC_CLK. One of the FPGA's DCMs (Digital Clock Managers) is used to adjust the phase of the parallel output data to meet this timing requirement. The FPGA is able to measure the timing relationship between the SYNC_CLK and the LSB of the parallel data (MD0) via IP_L32N and IP_L28N (at the upper right-hand corner of U401 on sheet 4 of 8.

The ±25 MHZ_FPGA source is used as the FPGA clock for pulse and blanking modulation. A DCM is used to multiply the 25 MHz clock to 200 MHz to provide 5 ns resolution for the pulse or blanking period and width. The FPGA can blank the RF and baseband outputs via the differential LVDS signals ±RF_BLANK and ±BB_BLANK.

The FPGA is initially programmed via the SPI from the CPU. Configurations are uploaded to the FPGA and stored in the flash ROM during system programming at the factory. A 6-pin JTAG connector, J400, allows direct access to the FPGA for development purposes.

Modulation ADC and DACs

(Schematic 8: Mother Board 5, Modulation ADC / DACs)

There is a rear panel modulation input BNC, J500, which allows user supplied signals to modulate amplitude, frequency, or phase of the SG384 outputs. The same input can also be used for pulse and blank modulation.

In EXT PULSE or EXT BLANK modulation modes, the rear panel modulation input is discriminated by U501 to provide a digital input, EXT_TRIG, to the FPGA. Depending on the operating mode and frequency, the FPGA will use EXT_TRIG to control ±RF_BLANK and/or ±BB_BLANK to pulse or blank the signal generator's outputs.

For EXT AM, FM or ΦM, the rear panel modulation input is limited by D501 & D502, buffered by U500A, ac or dc coupled through U503, and low-pass filtered by a 1 MHz, 5^{th} order, Bessel filter (L503/L504/C511-C514). The filtered signal is buffered by U504 and digitized by U502, a 12-bit ADC operating at about 31.25 MSPS. The data from the DAC is provided to the FPGA on the 12-bit parallel data bus, ADC[0..11]. The data is offset, scaled (and linearized in the case of amplitude modulation of RF outputs) and up-sampled to modulate the amplitude, frequency or phase of the signal generator outputs.

There are four high speed (125 MSPS), high resolution (14-bit) DACs that are controlled by the FPGA. The DACs have several purposes:

1. To mimic the modulation waveform on the rear panel modulation output BNC. 2. To level the RF amplitude during sweeps. 3. To level the baseband output during sweeps, or, to provide the I-component for I/Q modulation. 4. To level the doubler output during sweeps, or, to provide the Q-component for I/Q modulation.

All of the DACs have a similar configuration. The clock to each DAC is resynchronized to the PDCLK (from U605) to minimize sample jitter. The data to the DACs is loaded in parallel from the FPGA. The differential outputs are filtered by a Bessel low-pass filter (fc = 1 MHz for two of the DACs and fc = 10 MHz for the I/Q DACs). The filter outputs are buffered by differential line drivers with a fixed gain of ×2 and a 49.9 Ω source impedance.

RF DDS

(Schematic 9: Mother Board 6, RF Reference)

The RF DDS has two functions: To provide a reference frequency to the RF synthesizer (located in the RF block), or, in the case that the output is below 62.5 MHz, to synthesize the output directly. The RF DDS is an AD9910 (U605), which integrates a 1 GSPS NCO with a 14-bit DAC. The SFDR of the part is better than –65 dBc for output frequencies below 100 MHz. This is quite adequate for direct outputs (below 62.5 MHz) but would be unsatisfactory when multiplied up to higher frequencies. (For example, a spur would increase in magnitude by 40 dB when a reference is "multiplied" up from 40 MHz to 4 GHz.)

There is a neat trick to eliminate DDS spurs: If the DDS is programmed to divide by an integer, then the output will sample the exact same DAC levels on each cycle, and so each cycle will be the same as the others. Fourier tells us that a repetitive waveform can be represented by a fundamental sine and its harmonics; hence a *repetitive* waveform has only a fundamental and harmonics but no spurs. This is easily seen when observing a DDS output on a spectrum analyzer. As the FTW (Frequency Tuning Word) approaches a value that corresponds to division by an integer all of the spurs gather up fit beneath either the fundamental or its harmonics.

The requirement to divide by an integer requires further thought. For a 32-bit DDS, one cycle or 360° corresponds to 2^{32} = 4,294,967,296 in the phase accumulator. Division by an integer is simple if the integer is a power of 2. For example, to divide by 16 the FTW would be 4,294,967,296/16 = 268,435,456. However, to divide by 10, the FTW would be 4,294,967,29.6. Since the FTW must be an integer, there will be a truncation error of 0.6 bits per sample, a corresponding frequency error, and spurs in the output.

To fix this (in the case of division by 10) the DDS would be programmed to use a FTW of 429,496,729 for 9 sample clocks and 429,496,735 for 1 sample clock. Doing so accumulates exactly 2^{32} in the phase accumulator after 10 sample clocks and so provides exact division by 10 with no spurs. This trick allows the RF DDS to generate a reference frequency for the RF synthesizer that has no significant spurs and so can be "multiplied" by the RF synthesizer without adding spurs to the RF output.

The clock to the RF DDS comes from a 1 GHz VCO which is phase locked to ×51 the selected 19+ MHz reference to provide precision clock rates in the ranges of 997.259 MHz ±100 ppm, 1,000.000 MHz ±10 ppm, or 1002.7467 MHz ± 100 ppm. The charge pump output from the PLL synthesizer, U604, is filtered by U603, a low-noise, high bandwidth op-amp. The loop bandwidth is about 6 kHz.

The RF DDS is programmed to divide by an integer between 10 and 50 to provide output frequencies between 20 MHz and 100 MHz. The differential outputs are filtered and buffered before being sent to the RF Block to serve as the reference frequency input to the RF synthesizer.

The RF DSS has a 16-bit parallel port to allow for agile amplitude, frequency and phase modulation. The data is passed to the RF DDS from the FPGA modulation processor. The data on the parallel input, which is synchronized to the PDCLK, can directly modulate the amplitude or phase, or may be scaled and added to the FTW for FM. The DDS may also be rapidly modulated via the profile input ports, in which case the data is synchronized to the SYNC_CLK.

The data presented to the parallel port can only be used to modulate one parameter. In the case of frequency sweeps below 62.5 MHz, the parallel data provides frequency tuning data to the RF DSS. A separate path is used to amplitude level low frequency sweeps: The differential ±BB_LEVEL signal converted to a single-ended signal by U600 and used to level the amplitude of the RF_DDS synthesizer as seen at the front panel BNC output.

RF Block and Rear-Panel Options Interface

(Schematic 10: Mother Board 7, Interface)

The common mode voltage on the differential output from the RF DDS is eliminated by U700, which integrates the difference between the common mode output voltage and ground. The integrated voltage is applied to the 100 Ω terminations so as to eliminate the common mode voltage.

The differential DAC output is then filtered by a Chebyshev low-pass (L700, 701, 706, 707, etc) with a cutoff frequency of 150 MHz. The output of the filter is terminated and buffered by the differential amplifier, U702. A multiplexer, U701, passes the filtered RF DDS output to the RF block as either ±RF_REF (when the set frequency is above 62.5 MHz) or ±BB_OUT (when the set frequency is below 62.5 MHz).

The connector, J701, is used to pass signals between the motherboard and the rear panel options. Option 1 provides clock outputs at the set frequency. The RF signal required for this function comes directly from the RF block via an SMA cable, but power supplies and control signals (for controlling the amplitude and offset of the clock outputs) are provided via J701.

Option 2 provides a doubler to output a signal from 4 GHz to 8 GHz on a rear panel SMA connector. The RF signal required for this function comes directly from the RF block via an SMA cable, but power supplies and control signals (for controlling the amplitude of the doubler output) are provided via J701. Option 2 also provides a DC bias output on a rear panel SMA connector.

Option 3 provides rear panel analog inputs that can be used to directly modulate the I/Q modulator. The multiplexers U705 and U708 select between the internal I/Q modulation sources or the external I/Q modulation sources (which are provided by Option 3). This option also provides rear panel analog outputs which are copies of the I/Q modulation.

Power Conditioning

(Schematic 11: Mother Board 8, Power Supplies)

An enclosed power supply is used to provide regulated power the motherboard via the large header, J800. Whenever the unit is plugged into the line, the un-switched +24 V will be present. This supply is used to maintain power to the timebases (an OCXO or an optional rubidium oscillator) even when the front panel power button is "off". When the unit is switched "on" the other supplies (±15, ±5, +3.3V) become active. The inverter that generates those other supply voltages is operated at exactly 100 kHz, synchronized by the 100 ns wide, 200 kHz PS_SYNC pulses sourced from the CPU, U300.

The grounds and power supplies are all filtered and bypassed as they come onto the motherboard. In addition, there are several regulators which provide other voltages used in the system: +20, +8.5, +3.00 (which is used as a voltage reference throughout the system), +2.5, +1.8, +1.2, and –8.5 V.

An interrupt signal, –PWR_IRQ, is generated if the +24 V supply falls below +22 V or if the power switch is turned to "off". This interrupt tell the CPU to "stand down" (in particular to not start new writes to memory) as the power supplies are about to turn "off".

Motherboard to RF Block Jumper

(Schematic 12: Mother Board to RF Jumper)

This card provides the interface as well as filtering the signals to minimize any interference that could impair the signal quality. Single ended control signals implement a single order RC filter; differential signals implement a common mode choke; finally, power lines implement an LC filter.

This helps insure that the RF Output block and Motherboard do not interfere with each other.

RF Output Block

The RF Output Block refers to the milled aluminum block (and its covers) which house the type-N and BNC connectors which present the main front panel outputs of the instrument. This block establishes solid RF grounds, shields the enclosed circuitry from magnetic flux generated by the power supply and from RF signals generated by the motherboard, as well as reducing the EMI from and the susceptibility of the enclosed circuitry.

There are two circuit boards inside the RF block. Facing from the front of the instrument, the PCB on the right holds the RF synthesizer and provides connections to the motherboard via a 34-pin jumper board. The PCB on the left connects to the RF synthesizer and amplifies or attenuates the signal from the RF synthesizer. Signals on the type-N connector cover an amplitude range from –107 dBm to +13 dBm for signals from 950 kHz to 4.05 GHz. The output board also provides outputs on the BNC with an amplitude range from 1 mV_{rms} to 1 V_{rms} from dc to 62.5 MHz.

RF Synthesizer

(Schematic 13: Synthesizer 1, 2-4 GHz and Control)

Control signals, frequency references, and power supplies are passed from the motherboard via a small jumper board to the RF synthesizer on J101. Many of the control signals flow through to the output amplifier/attenuator board via J100. The ±8.5 V power supplies are re-regulated to ±5_SYN supplies by U100 and U111. Differential blanking signals, ±RF_BLANK and ±BB_BLANK are converted to CMOS levels by U117 and U118. Serial SPI data is clocked into the shift registers U112 and U113 to provide various control signals.

For output frequencies below 62.5 MHz the RF DDS direct output, ±BB_OUT, is used as the source frequency output. The differential signals are passed to the output board for conditioning before being applied to the output BNC connector. The differential signals are also buffered by U119 to provided sine wave outputs for type-N connector and discriminated by U120 to provide square wave outputs for the rear panel Option 1 & Option 2.

The RF synthesizer consists of a 1900-4100 MHz VCO, U105, which is phase locked by U107 to the RF reference (±RF_REF) from the motherboard. The differential RF reference is transformer coupled into the 100 MHz Butterworth low-pass filter (L102, C125 & C126) which is terminated by R116. The 3 V_{PP} reference is ac coupled into the PLL synthesizer's reference input into via C123. The charge pump output of the PLL synthesizer is conditioned by the loop filter, U104. The loop bandwidth is about 100 kHz for the typical phase comparison frequency of 25 MHz. The bandwidth of the loop filter, which is set to be roughly proportional to the phase comparison frequency, is adjustable by the switches U108A-D.

The output of the 1900-4100 MHz VCO is ac coupled into a high speed PECL fanout, U106. There are two sets of outputs from U106. The first output, ±TOP_OCT, is the differential top octave output for the frequency synthesizer. The other output is used as feedback to the PLL synthesizer and as is used to control the 50/50 symmetry of the top octave output.

The symmetry control is maintained by the differential integrator, U109. If +TOP_OCT spends more time high than –TOP_OCT, the inverting input to the integrator will ramp up, causing the non-inverting output of the integrator to ramp down, reducing the dc voltage at the non-inverting input of the fanout buffer, causing +TOP_OCT to ramp down, returning the symmetry of ±TOP_OCT to 50/50.

RF Dividers and Selectors

(Schematic 14: Synthesizer 2, Dividers and LPF)

The ±TOP_OCT PECL signals are fanned out by U200. Both outputs of the fanout are source-terminated with 50 Ω and can be made active by grounding the string of three series 50 Ω resistors on the open emitter outputs. (Pulling up these resistors to +3.3V turns "off" the corresponding open-emitter output.)

For outputs between 2 GHz and 4 GHz, –EN_RF0 is set low, enabling the top-half of the fanout U200. One of the differential outputs is selected by the RF multiplexer, U216, to drive the rear panel Option 1 & Option 2 via J201 (the SMA connector in the side of the RF Block). The other differential output of the fanout is used for the 2 GHZ to 4 GHZ output. This signal is given some high frequency pre-emphasis by the stubbed attenuator (R205-207), amplified by U201, then low-pass filtered by U202 (to remove the harmonics of the square wave) to provide a 2 GHz-4 GHz sine wave for RF multiplexer, U211, which passes the sine wave to the output amplifier/attenuator board via the RF feed-thru, J200.

For outputs between 62.5 MHz and 2 GHz, the control line –EN_1ST_DIV is set low, enabling the bottom half of the fanout, U200. (The top half is disabled by setting –EN_RF0 high.) This also enables the digital divider, U206, which will provide outputs via the gate U205 for outputs between 1 GHz and 2 GHz. Other dividers (U209, 212, 215, 218) are enabled for lower octaves. As before, each differential square wave source has a 50 Ω source impedance, with one-half of the differential pair being passed directly to the RF multiplexer, U216, while the other half is low-pass filtered to provide a sine to the other RF multiplex, U211. Unused dividers are disabled to eliminate sub-harmonic distortion.

The RF multiplexers (U211 & U216) are non-reflective multiplexers and so unselected inputs are terminated via 50 Ω to ground. These RF multiplexers operate with a VEE of –5 V_{DC} and so it is necessary to translate the control signals to swing between ground and –5 V_{DC}. A triple 1:2 analog switch, U213, is used to translate CMOS control signals to the 0 V/ –5V levels.

RF I/Q Modulator, Amplifiers and Attenuators

(Schematic 15: Output 1, Attenuation & Controls)

The PCB on the left side of the RF Block I/Q modulates, amplitude modulates, amplifies, and attenuates the selected RF signal before passing it out the front panel connectors. This PCB receives power, control and differential modulation signals from the RF synthesizer PCB via J101. The selected RF signal is passed from the RF synthesizer to this PCB via the RF feed-thru, J100.

The signal path toward the type-N connector begins at J100. If the carrier frequency is between 400 MHz and 4.05 GHz, the signal at J100 may be multiplexed to the I/Q modulator, U110. If the signal is outside of this range, or if I/Q modulation is not enabled, the SPDT switches, U103 and U104, bypass the I/Q modulator.

The carrier signal is ac coupled into the I/Q modulator via C116. The modulator converts the input signal into two phase-shifted square waves, I & Q. The each square wave can be amplitude modulated the corresponding differential modulation inputs, ±I_MOD and ±Q_MOD. The amplitude modulated components are summed together and appear at the RF output. The RF output is attenuated (to match its input carrier level), given high frequency pre-emphasis (via the stubs in the pi-attenuator legs) and low pass filtered (to remove harmonics) and directed back into the RF signal path by the SPDT switch, U104.

Two RF voltage variable attenuators (VVA), U111 & U112, are used to amplitude level or amplitude modulate the RF signal. The attenuation is controlled by a dc voltage applied to the V1 input of each VVA. The attenuation increases as V1 becomes more negative. The attenuation characteristic is not linear, which requires compensation to the control voltage, especially for deep amplitude modulation.

The attenuator control voltage is sourced from ±RF_ATTN, which is converted to a single-ended voltage by U114 and low-pass filtered (for noise reduction) by L106 and C128. These attenuators are used to provide attenuation between the digital attenuator steps and to correct for the differential non-linearity of the digital attenuators. They are also used to amplitude level sweeps and for amplitude modulation.

The first of three RF gain blocks is U109. The gain of this amplifier is +15 dB. It is an ac amplifier which requires a dc current bias be applied to its output. It is important that the dc bias network be high impedance over the operating range (1 MHz to 4 GHz) and that it not have any significant resonances. This is achieved with three series inductors, with staggered self resonant frequencies, and with parallel damping resistors. This method is used on all the gain blocks in the signal chain.

The output from the first gain block is ac coupled into the first of five digital attenuators, U107. The digital attenuators are controlled in 0.5 dB steps from 0 dB to 31.5 dB. They are powered from +5 V and are controlled by the SPI interface. The power supplies and SPI signals are filtered from stage-to-stage to reduce signal and noise feed-through.

RF Output Attenuators

(Schematic 16: Output 2, RF Stage)

To achieve an amplitude dynamic range of 120 dB (from –107 dBm to +13 dBm) at 4 GHz requires extraordinary care in the design, layout and grounding of the circuit. In particular, it is important that there be no signal paths which "go around" the intended signal path. For example, if –100 dB of a signal can go around the attenuator chain via a control line or power line, then the effective attenuation range will be limited.

RF grounding is reestablished in each of the four stages shown on Sheet 2 of 3, with both the power supplies and serial control lines being filtered at each stage before being passed to the next. Even the signal from U201 (which detects the output power) is filtered as it returns back to the front of the RF signal chain. Physically, the circuit layout is within a series of "rooms", with good ground connections, and shielded from other parts of the circuit by the milled aluminum block.

The RF signal chain continues with the output of the attenuator on the previous page being applied to the first attenuator, U201, on the next page. The signal chain continues with an amplifier, two attenuators, another amplifier, and a final output attenuator. The final amplifier, U206, has higher gain and can provide more output power than the other gain blocks. It also requires more bias current.

There is an RF power detector, U207, positioned directly at the type-N output connector. This detector cannot be used for absolute calibration, but is useful for turn-on testing, and the measurement of the differential nonlinearity of the digitally controlled attenuators.

BNC Output

(Schematic 17: Output 3, BNC)

The differential outputs, ±BB_OUT, are passed from the RF DDS on the motherboard to the output board via the RF synthesizer board. These differential signals can be blanked by the dual differential switches U301 & U302 by BB_BLANK_CTL.

±BB_OUT are converted to a single-ended signal by U303, whose output is low-pass filtered (to reduce noise bandwidth and reduce high frequency spurs) by L303, C305 & C306. The signal is then attenuated by the digitally controlled attenuator, U304, which can provide 0 to 31 dB of attenuation in 1 dB steps. (Finer steps are provided by the RF DDS, whose amplitude can be set with 16-bit of resolution.) A fixed 30 dB of attenuation is provided by R302/306/307 under the control of the switch U305. The high bandwidth switches, U301, U302 and U305, are operated from ±3 V, and so their control lines are level shifted by U100 and U101 to ±3 V.

An output amplifier, U300B, buffers the attenuator output and provides a gain of ×3. A final output driver, U300A, sums in an offset voltage, BB_OFFSET, and drives the output BNC via a 49.9Ω resistor. The BNC output is sampled for measurement by the CPU via the filtered signal BB_MON.

Power Supply

(Schematic 18: Power Supply)

The power supply for the unit is contained in a separate shielded enclosure. The unit accommodates universal input voltages (90-264 V_{AC}, 47-63 Hz) and provides a variety of dc voltages to the motherboard (+24, +15, +5, +3.3, –5, –15 V.) The unit will lock its dc-dc converter to a 200 kHz sync signal provided by the motherboard. The unit also has a thermostatically controlled fan whose speed increases with increasing temperature.

An OEM power supply (CUI Inc VSBU-120-24) provides up to 5 A at +24 V from the line voltage input. This power supply is "on" whenever the line voltage is present, supplying +24 V to the motherboard to power the timebase (either the standard ovenized crystal or optional rubidium oscillator.) The +24 V supplied to the motherboard is filtered by L1 & C1 to remove ripples from the OEM power supply. The OEM supply also provides +24 V for a dc-dc converter to generate the other regulated voltages used in the system. The dc-dc converter and fan are "on" only when the front panel power button is pressed "in".

The dc-dc converter is disabled when the –DISABLE (pin 8 on the motherboard interface) is held low. When –DISABLE is released the switching power supply controller, U7, generates complimentary square waves at about 100 kHz to drive the MOSFETs (Q2 & Q3) into conduction during alternate half-cycles. The MOSFETs drive the primary of a transformer. The secondary voltages are rectified, filtered, and regulated to provide the +15, +5, +3.3, –5, & –15 V system voltages.

The regulated outputs have Schottky diodes on their outputs which prevent the power supplies from being pulled to the wrong polarity by loads which are connected to other supplies with opposite polarities. This is most important during start-up and to avoid SCR action in CMOS ICs in the case that one of the supplies should fail.

A thermostatic fan speed control helps to regulate the operating temperature of the entire instrument. This circuit uses an LM45 (10mV/deg C) as a temperature sensor. The output from the temperature sensor is offset, multiplied, and limited to a 0-15 V range. This voltage is drives a 12 V medium speed fan via the emitter follower, Q1.

Rear-Panel Options

The SG384 provides three options that extend the performance of the instrument. All rear panel options interface to the mother board via the Option Jumper PCB (Schematic 19: Rear Panel Option Jumper).

Clock Output (Options 1)

(Schematic 20: Option #1 Clock Outputs)

These options are located on small boards attached to the rear panel and connected to the motherboard by a small vertical board which supplies power and control signals. The SPI is used to transfer serial data to a quad DAC and an octal shift register. A square wave at the RF frequency comes to the option PCB directly from the RF block via a coax cable with SMA connectors. This signal is the source for the rear panel clock and doubler outputs.

The RF square wave is terminated and fanned out by U110. One differential pair is used to drive the RF doubler and the other provides a clock to a laser diode driver, U109, which in turn drives the rear panel differential clock outputs.

The clock outputs have adjustable amplitude and offset which are controlled by two 12-bit DACs in U100. Since the power supply rails for the laser diode need to move with respect to ground as the offset is changed, the RF inputs need to be ac coupled. However, since the clocks need to work down to dc, the levels need to be dc restored after the ac coupling. The signal is ac coupled via C113 & C114 and the four transistors, Q102A&B and Q103A&B, provide the dc restoration. Gains and time constants are set so that all the parts work together as a high speed level shifter.

The laser diode driver switches a constant current source between the ±OUT. The magnitude of this current source (and so the amplitude of the clock output) is adjusted by the voltage at the MODSET input. This voltage is set by the AMPL_CTL output from the DAC, level shifted by the current mirror, U101B and Q100A&B.

The offset of the clock output is controlled by V_HIGH, which has been offset and scaled by U101A from the DAC output OFFS_CTL. The pull-up resistors for ±OUT are connected to a potential equal to 2.33×V_HIGH as sourced by the regulator U106. The regulator only works properly when sourcing current, which would be a problem for negative offsets. The transistor pair Q104A&B assure that the regulator will source current by turning “on” for negative offsets.

The ±OUT from the laser diode driver are coupled to the rear panel clock outputs via a – 8.5 dB attenuator (R113-R121) which also allows for the insertion of an output offset. The layout is important to maintain high bandwidth as the transition times of the clock outputs are about 35 ps or 12 GHz. The clock outputs are sensed by R117 and R111 and offset, scaled, filtered and returned to the motherboard’s CPU’s ADC via the multiplexer, U105. This allows the microcontroller to do a system check on power-up as well as course offset and amplitude calibration.

RF Doubler (Option 2)

(Schematic 21: Option #2 4-8 GHz Doubler)

The rear panel Option 2 can provide RF sine wave outputs from 4.05 GHz to 8.10 GHz with amplitudes from +7 dBm to –20 dBm. When enabled (by asserting EN_DBL), the RF gain blocks are biased "on", enabling the RF output.

The signal path starts with the RF differential square wave, ±RF. The +RF is low-pass filtered (to remove the square waves odd harmonics) and ac coupled into the gain block U205. The gain block increases the signal by 15 dB to drive the doubler, U209, which is a passive doubler with about 16 dB of insertion loss. The output of the doubler is ac coupled into the voltage variable attenuator (VVA), U210, whose attenuation level is controlled by the voltage applied to its V1 input.

The differential signal, ±DBL_LEVEL is converted to a single-ended signal by U213, whose output is low-pass filtered by L210 and C226, and applied to the VVA's control input. The VVA is used to set output levels with higher resolution than allowed by the digital attenuator which follows, and to level output amplitudes during sweeps.

The output of the VVA is ac coupled into the gain block U206, which provides about 12 dB of gain. The output of that amplifier is ac coupled into the digital attenuator, U211, whose attenuation can be set in 0.5 dB steps from 0 dB to 31.5 dB. The attenuator is controlled by 6 bits from a shift register (U216) which is operating between 0 V and –5 V to level shift the control bits to the proper level for the digital attenuator. Serial data, clock and register strobe are level shifted from CMOS levels to 0 V & –5 V by the triple 2:1 analog switch, U215. Serial data out of the shift register is level shifted by R229 & R230 and buffered by U214 to return the data loop to the CPU for testing purposes.

The output from the digital attenuator is ac coupled into the gain block U207, which provides about 12 dB of gain. The output from this gain block is ac coupled to the SMA output connector, J201. The RF is detected by U204, at the final gain block for power-on testing and to calibrate the differential non-linearity of the digital attenuator.

Option 2 also provides a $\pm 10\ V_{DC}$ bias output on a rear panel SMA connector via a 50 Ω resistor. This output is controlled by the DAC output DC_OUT which may be set from the front panel. User loads should not exceed 20 mA on this output.

I/Q Modulator (Option 3)

(Schematic 22: Option #3 I/Q Modulator)

Option 3 provides for rear panel I/Q modulation inputs. These inputs allow the user to modulate the amplitudes of the in-phase and quadrature components of RF carriers between 400 MHz and 4.05 GHz with analog signals.

The I & Q channels use the same circuit configuration. The quadrature component, ±0.5 V or 1 Vpp, is applied to the rear panel BNC connector, J2. The input signal is terminated into 50 Ω by the parallel combination of the 52.3 Ω input termination in parallel with the 1125 Ω input impedance to the differential amplifier U4. The differential outputs drive a differential transmission line returning to the motherboard via 49.9 Ω resistors and J4.

Overloads are detected at the output of the differential amplifier by the fast window comparator, U2A&B. If an overload is detected at either the I or Q inputs, the differential signal ±OVLD_I/Q will be asserted and passed to the motherboard via J4 for detection by the CPU.

This option also provides rear panel I/Q modulation outputs. The modulation signals may originate from the rear panel modulation input (Option 3) or from the internal, dual, arbitrary modulation generator (to be implemented in future products). The modulation signals from the motherboard, ±I_OUT and ±Q_OUT are received by U1 and U5 and converted to single-ended signals which drive the BNC outputs via 49.9 Ω resistors. These outputs are intended to drive 50 Ω loads to ±0.5 V or 1 V_{pp}.

Timebase Options

(Schematic 23: Timebase Adaptor Interface)

The standard timebase is an OCXO (SRS p/n SC-10-24-1-J-J-J-J). A rubidium frequency standard (SRS p/n PRS10) may be ordered as Option 4. Both timebases are held by the same mechanical bracket and connected to the system using the same adapter PCB.

The adapter PCB schematic is quite simple: J1 is the connector to the OCXO option, J2 is the connector to the rubidium option, and J3 is the connector to the main PCB. The op amp U1 is used to scale the 0-4.095 V_{DC} frequency calibration voltage (CAL_OPT) to 0-10 V_{DC} for the OCXO or 0-5 V_{DC} for the rubidium. The logic inverter, U2, is used to invert the logic levels for the RS-232 communication between the microcontroller on the main PCB and the PRS10 rubidium frequency standard.

Appendix A : Rational Approximation Synthesis

The SG300 Series RF synthesizers use a new approach to synthesizer design that provides low phase noise outputs with virtually infinite frequency resolution and agile modulation characteristics. The technique is called Rational Approximation Frequency Synthesis. Some details of the technique will help users to understand the performance capabilities of the instruments.

Phase Lock Loop Frequency Synthesizers

Phase lock loop (PLL) frequency synthesizers are a cornerstone technology used in every modern communication device and signal generator. The classical PLL block diagram is shown in Diagram 1.

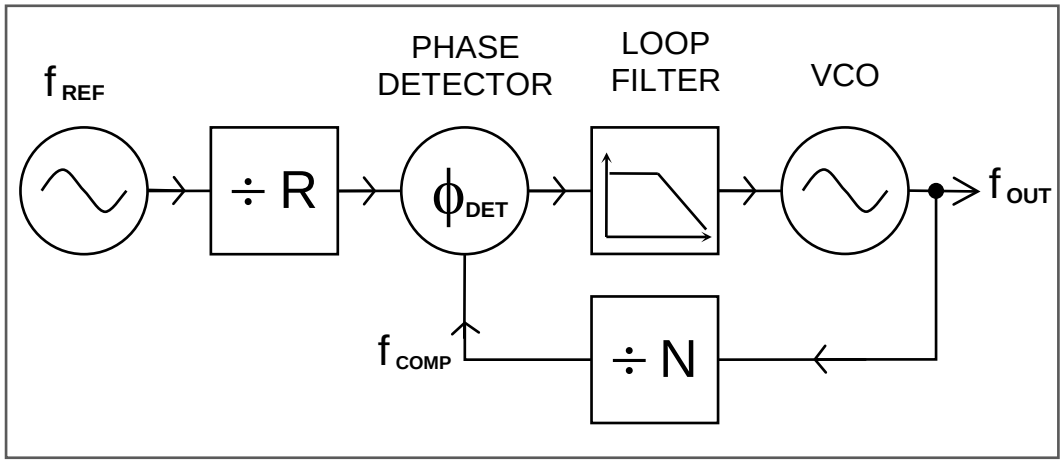


Diagram 1: Classical "Integer-N" PLL Frequency Synthesizer

The purpose of the PLL synthesizer is to generate precise output frequencies that are locked to a reference frequency. As shown in Fig 1, the reference frequency, f_{REF}, is divided by the integer R and the voltage controlled oscillator (VCO) output, f_{OUT}, is divided by the integer N. A phase detector compares the phase of the divided frequencies. The phase detector output is low-pass filtered and used to control the frequency of the VCO so that f_{OUT} / N is equal to f_{REF} / R, hence $f_{OUT} = N \times f_{REF} / R$.

A numerical example will help to illustrate the operation and design trade-offs of the PLL. Suppose f_{REF} = 10 MHz and R = 1000. If N = 10,000 then the output frequency, $f_{OUT} = N \times f_{REF} / R$ = 100 MHz. As N is changed from 10,000 to 10,001 to 10,002, f_{OUT} will change from 100.00 MHz to 100.01 MHz to 100.02 MHz. This PLL synthesizer has a phase comparison frequency, and a channel spacing, of f_{REF} / R = 10 kHz.

Phase Noise

Diagram 2 shows a typical phase noise plot for a 100 MHz PLL synthesizer. The phase noise plot shows the noise power in a 1 Hz sideband as a function of frequency offset from the carrier. There are three dominate sources of phase noise: The reference, the phase detector, and the VCO. The frequency reference dominates the noise close to the carrier but falls off quickly at large offsets. The phase detector noise floor is relatively flat vs. frequency but decreases with increasing phase comparison frequency. In fact, the phase detector noise decreases by about 10 dB / decade, hence is about 30 dB lower for phase comparisons at 10 MHz vs. 10 kHz. Finally, the VCO phase noise will dominate at offset frequencies beyond the loop bandwidth. A high phase comparison frequency, hence low R & N divisors, is required for a low phase noise design.

In a properly designed PLL the output noise tracks the reference at low offsets, matches the phase detector noise at intermediate offsets, and is equal to the VCO noise at offsets beyond the PLL loop bandwidth. Careful attention to the loo`p filter design is also required to achieve the total noise characteristic shown in Diagram 2.

In addition to broadband noise there will be discrete spurious frequencies in the phase noise spectrum. A dominant spur is often seen at the phase comparison frequency. It is easier to reduce this spur in a filter when the phase comparison frequency is high.

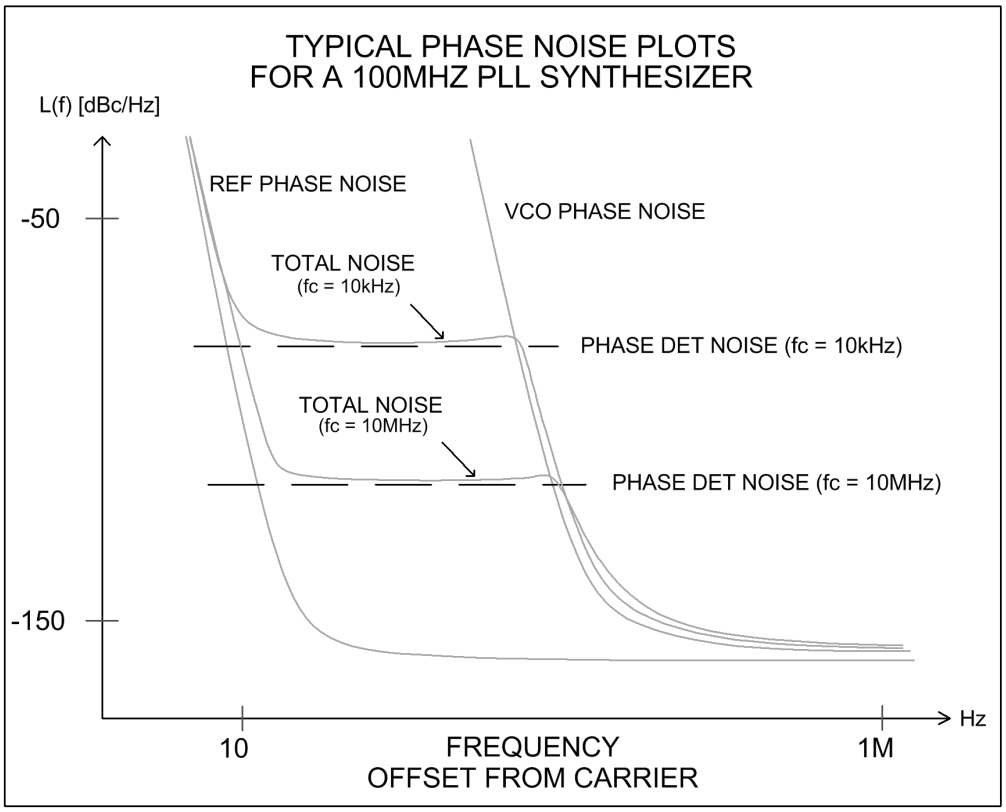


Diagram 2: Typical Phase Noise Spectrum for a 100 MHz PLL Frequency Synthesizer

Increasing Frequency Resolution

A frequency resolution of 10 kHz, or channel spacing of 10 kHz, is adequate in many communications applications but a higher resolution is desired in test and measurement applications. The simplest way to increase the frequency resolution is to increase the value of the R divider. In the above example, if R were increased from 1000 to 10,000 the frequency resolution (channel spacing) would be increased from 10 kHz to 1 kHz. However, there are several serious drawbacks to this strategy. As the R divider is increased the phase comparison frequency is decreased leading to higher phase detector noise, a reduction in the loop bandwidth, and increased settling times. *Increasing R will achieve high frequency resolution at the cost of a noisy output that takes a long time to settle.*

A Note on Fractional-N Synthesis

Another strategy to increase resolution without decreasing the phase comparison frequency is to use a Fractional-N synthesizer. In these synthesizers the value of N is modulated so that its average value can be a non-integer. If N averages to 10,000.1 then the output frequency, $f_{OUT} = N \times f_{REF} / R = 100.001$ MHz. The frequency resolution has been improved to 1 kHz. However, modulating the N value creates spurs in the VCO output. Dithering techniques are able to spread most of the spur energy into broadband noise, but the remaining noise and spurs is problematic in some applications.

About YIG Oscillators

One work-around to the trade-off between high resolution and reduced phase comparison frequency (and so higher phase noise) is to use a YIG oscillator. YIGs are extremely good VCOs due to the extremely high Q of their resonator which consists of a sub-millimeter yttrium-iron-garnet sphere tuned by a magnetic field. However, YIGs have their drawbacks including high power, slow tuning, susceptibility to environmental magnetic fields, and high cost. The SG300 Series of RF synthesizers achieve YIG performance from electrically tuned VCOs by arranging a very high phase comparison frequency.

A New Approach

A new approach to synthesizer design provides high frequency resolution, fast settling, and low phase noise. This new approach is called *Rational Approximation Frequency Synthesis*. (A rational number is a number which is equal to the ratio of two integers.) The approach has been overlooked as it relies on some surprising results of rather quirky arithmetic which abandons neat channel spacing in exchange for a much better performing PLL synthesizer.

Once again, a numerical example will be useful. Suppose we want to use our PLL synthesizer to generate 132.86 MHz. We could do that by setting R = 1000 and N = 13,286. With f_{REF} = 10 MHz we have $f_{OUT} = N \times f_{REF} / R$ = 132.86 MHz. The phase comparison frequency is 10 kHz and so the PLL loop bandwidth, which is typically $1 / 20^{th}$ of the phase comparison frequency, would be only about 500Hz.

There's another way to synthesize 132.86 MHz (or at least very close to it.) Suppose we set R = 7 and N = 93. Then $f_{OUT} = N \times f_{REF} / R$ = 132.857142 MHz, which is only 21.5 ppm below the target frequency (Hence the term "Rational Approximation". Of course, increasing the reference frequency by 21.5 ppm will produce the target frequency exactly, as will be described.) Momentarily suspending the question of the general applicability of this approach, the positive benefit is clear: The phase comparison frequency is now 10 MHz / 7 = 1.42 MHz which is 142 times higher than that provided by the classical PLL with a 10 kHz channel spacing. This allows a PLL bandwidth which is also 142 times wider. The higher comparison frequency of this PLL will provide faster settling, lower phase noise, and an easily removed reference spur which is 1.42 MHz away from the carrier.

Several questions arise.

1. Is this approach generally applicable, that is, can *small* values for R & N always be found to produce an output close to any desired frequency?
2. Is there a method to find the smallest values for R & N?
3. Can the output frequency be made exact (not just "close to") the desired frequency.

The answer to all three questions is "Yes". Details are well illustrated by a real-world example.

An Example

Diagram 3 shows a PLL synthesizer that can generate outputs anywhere in the octave between 2 GHz and 4 GHz. Lower frequencies are easily generated by binary division of this output. This example uses an Analog Devices dual-modulus PLL frequency synthesizer, the ADF4108. A dual modulus N counter is a high-speed divider which divides by a prescaler value, P, or by P+1 under the control of two registers named A & B. The dual modulus N-divider adds a bit of numerological quirkiness as there are restrictions on the allowed values for A & B as detailed in Diagram 3. The ADF4108 also requires that the phase comparison frequency be less than 104 MHz. The reference frequency input in this example is 200 MHz.

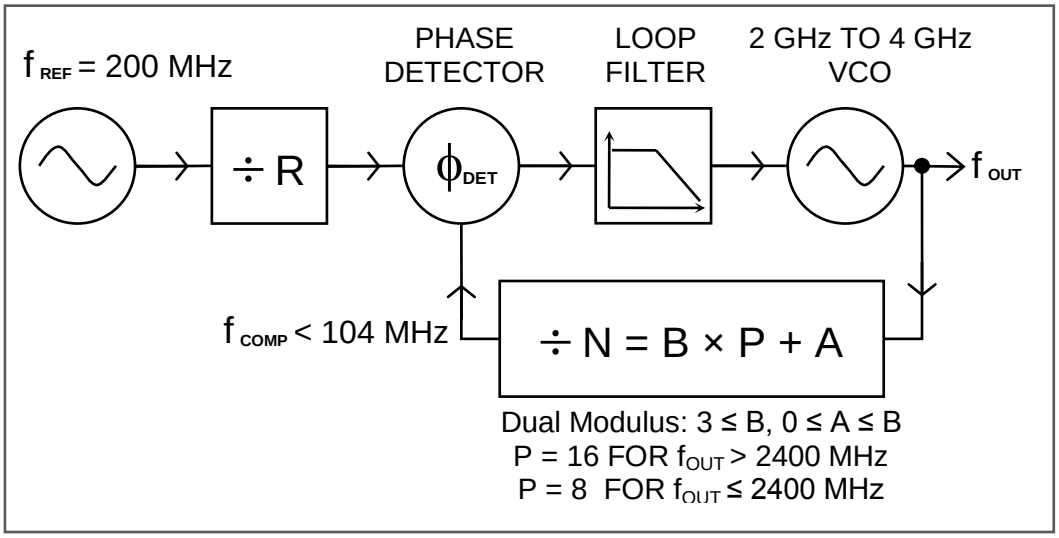


Diagram 3: A Rational Approximation Frequency Synthesizer

One curious aspect of Rational Approximation Frequency Synthesis is that it is not obvious how to choose the values for R & N. There are mathematical techniques for rational fraction approximation however brute enumeration of the possibilities may also be used. For example, R & N can be found by starting with the lowest allowed value for R and testing to see if there is an allowed value for N which gives a result, $f_{OUT} = N \times f_{REF} / R$, which is within some error band (say, $\pm$100 ppm) of the desired frequency. Luckily, these computational requirements are modest. The required calculations can be performed on a typical microcontroller in under a millisecond.

The largest phase comparison frequencies are achieved when there are many numeric choices available to improve the chance that a particular ratio of integers can be found which will be within the error band of the desired result. This is done three ways. First, allow a large error band. (An error band of $\pm$100 ppm is typical because a fundamental mode crystal oscillator, which is used to clean-up the reference source, can be tuned over $\pm$100 ppm.) Second, use a high frequency reference oscillator. Third, provide a second reference, detuned slightly from the first, to provide additional numeric choices.

To ascertain how well Rational Approximation Frequency Synthesis works for the example in Diagram 3, a computer program was written to compute the R & N values for 10,000 random frequencies in the octave band between 2 GHz and 4 GHz. Using a single reference source at 200 MHz, and an allowed error band of ±100 ppm, the average phase comparison frequency was 9.79 MHz and the worst case phase comparison frequency was 400 kHz.

When a second reference frequency was available (at 201.6 MHz, as determined by trial and error while searching for the highest worst-case phase comparison frequency) the average phase comparison frequency increased to 12.94 MHz and the worse case phase comparison frequency increased to 2.35 MHz (a six-fold increase.)

Elimination of Error

Rational Approximation Frequency Synthesis provides a fast settling, low phase noise, and spur-free output, but with a troubling "error band" of typically ±100 ppm. To eliminate this error it will be necessary to provide a low noise reference that is tunable over ±100 ppm with very high resolution. A VCXO phase locked with narrow bandwidth to a DDS source may be used for this reference. A 48-bit DDS provides a frequency resolution of $1{:}2\times10^{-14}$ and the VCXO effectively removes all of the DDS spurs.

A tunable reference source is shown in Diagram 4. A 10 MHz timebase in multiplied in the DDS to 100 MHz. The DDS is programmed to generate an output within ±100 ppm of 18.1818 MHz. The VCXO is phase locked to the DDS output with a 100Hz bandwidth. The clean 18.1818 MHz VCXO output is used as a source for an 11× multiplier to produce a 200 MHz reference tunable over ±100ppm with a frequency resolution of $1{:}2\times10^{-14}$. This tunable frequency reference is used as the reference for the Rational Approximation Frequency Synthesizer, eliminating the error band inherent in the technique.

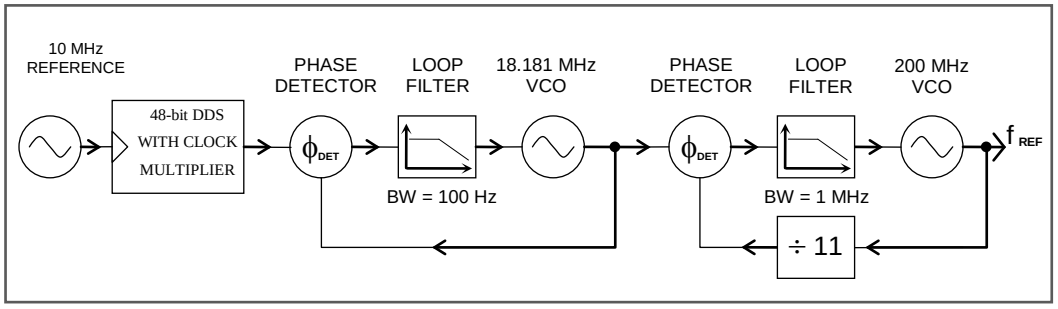


Diagram 4: Tunable (±100 ppm) 200 MHz Reference

Conclusion

A new method for the operation of classical integer-N PLL frequency synthesizers has been described. The method, Rational Approximation Frequency Synthesis, allows for operation at much higher phase comparison rates than the classical approach. The higher phase comparison rates allow wider PLL bandwidth to provide faster settling, lower phase noise, and spur-free outputs with virtually infinite frequency resolution.